EDN europe

Mapping transfer efficiency for wireless power

pulse

designideas

COVER

Real-world measurements on wireless-power-transfer designs

Keysight Technologies has introduced wireless power transfer software, that provides real-time power transfer efficiency measurements, accurately characterising wireless power transfer devices; measuring power transfer efficiency in real time; and testing to wireless power transfer standards. A key factor in designing WPT devices is the performance of the power transfer efficiency between coupled coils and resonators, leading to need to characterise these components and measure power transfer efficiency in real-time. Keysight's new WPT analysis option provides that capability with its arbitrary load impedance setting. Keysight adds, "Performing this testing according to wireless power transfer standards is just as critical. For today's product integrators, component manufacturers and test centres, this new software option means they now have the functionality needed to properly test their WPT devices and wireless charging systems." The wireless power transfer analysis option is for several of Keysight's ENA series network analysers, enabling those instruments to address the needs of emerging wireless power transfer (WPT) markets. A feature of the WPT analysis software is its ability to enable network analyser users to perform advanced 2D/3D simulation. Doing so allows them to visualise the dependency of load impedance in wireless power transfer systems, as depicted by the 'surface' in the image. More here.

FEATUREARTICLES

ONLINE THIS MONTH

EDN's columns

Make No Compromises

Increase Your Design's Functionality with 8-bit PIC® MCUs

Timing and Counting

Human Interface

System and Safety Management

Power Conversion and Charging

8-bit PIC® MCU Core

Output and Signal Generation

Input and Sensor interface
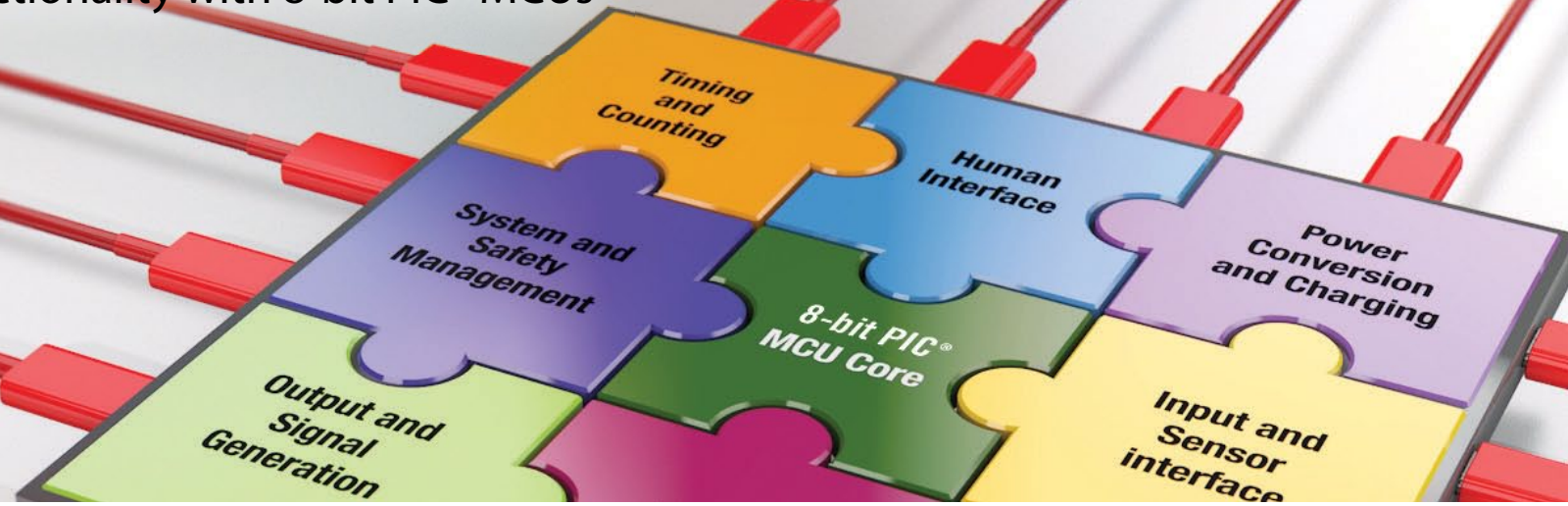
In embedded system design, reality demands that compromises are made at every phase. Tradeoffs between performance, functionality and cost often prevent you from bringing your best ideas to market. We believe there's a better way. That's why we've architected our latest 8-bit PIC® microcontrollers (MCUs) with flexible, "core independent" blocks of hardware intelligence that react quickly, consume very little power and are much more code-efficient than a software-based approach. In essence, Core Independent Peripherals help you easily combine many complex system functions onto a single MCU, increasing speed and flexibility, while reducing power consumption and cost. Design with 8-bit PIC MCUs, and you won't have to compromise.

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THE VW SAGA

For all the hours of air-time, and hectares of print journalism, that have already been devoted to the Volkswagen emissions-testing scandal, there is a great deal we don't yet know, and quite possibly, never will. For example; were we able to reach deep into the design groups at VW, would we find a team that viewed what it was doing as fundamentally wrong, immoral, illegal, and was writing its code in the full knowledge of what was likely to happen if (or, as it has turned out, when) they were discovered?

Or would we find a mindset that didn't regard what it was doing as anything remarkable; "this is what we have to do to pass the tests; they're only a formality; many car makers do something like this; everyone knows that real-world performance is nothing like the rolling-road test"? If it is the latter, the rules of the schoolyard have been made clear. "Everyone does it," is no defence when you are caught out in the open, doing the same deed in full view. One question that has yet to be answered, at least as far as I know, can be framed thus; It is clear that the engines can be made to meet the specified emission limits. What, in that case, is the performance, or specification, restriction that would result from simply placing the ECU in "test scenario mode" (my terminology) – all the time? Is it marginal, or substantial? Does it impact driving performance (rev limits, BHP, torque?) or does it mainly affect fuel economy?

This last point is almost a given, if for no other reason that NOx production is greatest at higher fuel-burn/cylinder head temperatures, whereas fuel economy improves at higher temperatures: and concentrations of NOx have grabbed most headlines in the VW episode. Or is it the case that real-world driving conditions simply cannot be faithfully reproduced in a test suite (which seems improbable) and that on-the-road results are always going to be worse than in-the-lab?

There's a grave danger of demonising an industry that has achieved, and surpassed, many objectives set for it, and that it has set itself. Efficiency and performance, and perhaps most of all, safety, are so far ahead of the standards of only two or three decades ago as to be almost unrecognisable. Nor should we be unduly condemning of the Diesel engine. Some of the most vocal commentators of the last few weeks might remind themselves that without Diesel powered agricultural machinery, the world would starve in short order; international trade (shipping) would cease; and almost all land transport other than passengers cars (and electrified trains) would come to a halt. Transport – especially, moving people, because the ratio of mass-of-vehicle to mass-of-cargo is always unfavourable – is inherently costly, including in environmental costs. This present scandal hinges on the fact that the Diesel engines have been found to be imposing that environmental cost where it is most harmful – on city streets. The cost will manifest itself at some point. Today's "ultimate solution" is the electric car (EV or plug-in hybrid). Which would be a fine option if they were backed by, and powered by, a network of renewable resources or nuclear power stations. Renewables are a long way from providing the necessary generation base; and several territories where EVs are progressing are turning away from nuclear. Which leads to the harsh fact that most of today's EVs are in reality powered by coal – or at best, natural gas. Although the emissions are out-of-town.

That in itself may be an acceptable tradeoff, but it becomes a political decision. Therefore, we can say to policy makers; the automotive industry has demonstrated that it can do great things for you, and meet seemingly-impossible targets; but there are fundamental limits. If you "squeeze the balloon" too hard in one place, it will expand in another direction. You will want to impose some sanction on VAG for its transgression but this is not an issue that justifies permanently damaging the company. It is, after all, delivering product that is massively better than the equivalent of a few years ago: just not as good as the nominal specification required.

And, automotive software coders; it's probably best not to try that one again.

pulse
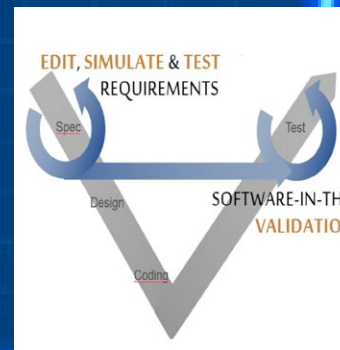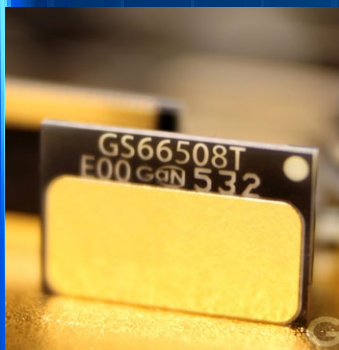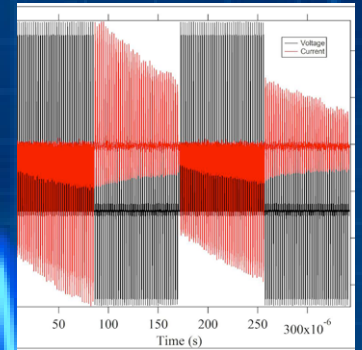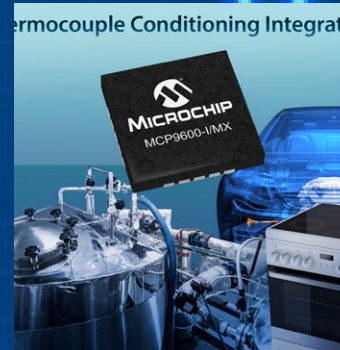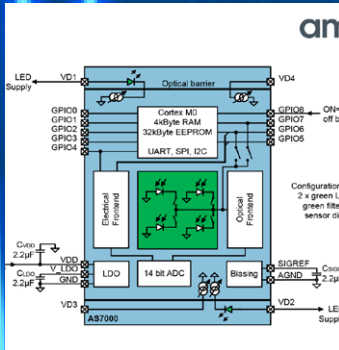
Programmable multi-channel transceiver for sub-GHz designs

Melexis' MLX73290-M is a multi-channel, low power RF transceiver IC addressing the sub-GHz ISM bands from 300 to 960 MHz: it has two RF channels, each with a programmable RF PA and a sensitive RF receiver. It is fully programmable via its serial peripheral interface (SPI) and includes energy harvesting interface and transmit power detectors.

This IC is, according to Melexis (Tessenderlo, Belgium), suited to sub-GHz wireless applications such as home/building automation, tyre pressure monitoring (TPMS), automatic meter reading (AMR), alarm systems, passive keyless entry (PKE), medical diagnostics and telemetry. Its output power level ranges from -20 dBm to 13 dBm while its receiver sen-sitivity can reach -120 dBm in a 15 kHz bandwidth. Maximum data rate is 250 kbps. A wide variety of different RF parameters can be adjusted (number of channels, frequency resolution, output, frequency deviation, etc.), in order to satisfy specific application criteria. On-off keying (OOK), binary frequency shift keying (FSK), minimum shift keying (MSK), Gaussian minimum shift keying (GMSK) and Gaussian frequency shift keying (GFSK) modulation schemes are supported.

Two RF power detectors provide augmentation of radiated power performance during transmission. An energy harvesting interface allows battery-less power supply by using a solar cell in combination with a super capacitor. Evaluation boards and software tools are also available. In a 5 x 5 mm 32-lead QFN package, it operates over -40°C to 105°C.

Complete article, here ▶

Multifunction biosensor/vital signs monitor for wearables, from ams

Sensor and mixed-signal IC specialist ams (Graz, Austria) has applied optical detection techniques to produce a sensor capable of accurate heart rate measurement; the company says its device is the first "total solution for 24/7 heart rate measurement for wearables".

AS7000 is the first in what is to be a family of health/fitness solutions from ams, for wearable devices. The AS7000 solution incorporates a highly integrated optical sensor module accompanied by software to provide the highest accuracy optical heart rate measurements (HRM) and heart rate variation (HRV) readings, backed by opto-mechanical design-in support. The 24/7 reference is to indicate that ams intends the device for prod-

ity measurements by providing interfaces to external sensors.
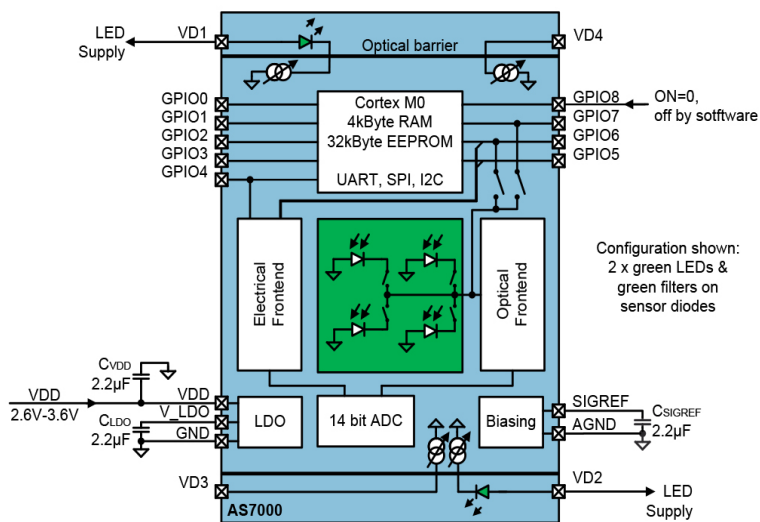
The operation of the AS7000 is based on photoplethysmography (PPG), an HRM method which measures the pulse rate by sampling light modulated by the blood vessels, which expand and contract as blood pulses

ucts that are worn continuously, rather than (for example) only during periods of exercise. The device delivers a processed output in beats per minute, updated once per second.

The module includes the LEDs, photo-sensor, analogue front end (AFE) and controller as well as application software required to implement an accurate optical HRM/HRV fitness band product. The module also accommodates skin temperature and skin resistiv-

through them. Unlike existing optical AFEs, which produce raw PPG readings, the AS7000 integrates a digital processor which implements algorithms developed by ams.

ams observes that deriving accurate and reliable data from the raw measurements in this domain is far from simple. The variation in returned light that is due to expansion and contraction of blood vessels is, in effect, a small AC signal superimposed on a large

DC component: around two orders of magnitude difference. Motion, including that due to the heartbeat itself, introduces a further "error" source of motion artifacts, that can be removed by adding an accelerometer (external to the AS7000).

At its introduction, the AS7000 outputs heart rate data; software can follow trends in the HRM data to derive HRV parameters. Skin temperature and resistivity (GSR, galvanic skin resistance) parameters will be added (via software), and ams also has a feasibility study looking at blood pressure monitoring. This can, in principle, be derived from the transcutaneous optical measurement, the company says, but is an even more challenging signal processing task. The same

is true for SPO_2, or (reflective) oxygen saturation measurement, and that, too, is on the company's roadmap for the product range. The AS7000's low-power design is aimed application in fitness bands, smart watches, sports watches, and devices in which board space is limited and in which users look for extended, multi-day intervals between battery recharges. The processor core is an ARM Cortex M0.

Complete article, here

Open source pocket USB oscilloscope; 30 MHz, multi-platform

Running on Apple iPad, Android, Microsoft Windows and Linux, LabNation's (Antwerp, Belgium) open source USB oscilloscope, SmartScope, is the result of a Kickstarter campaign commenced in 2014. Believed to be the first test equipment designed to run on multiple operating systems and platforms such as smartphones, tablets and PCs, the lightweight SmartScope is powered directly from the host's USB interface suiting it for many test and measurement applications far from the workbench.

SmartScope combines the multiple functions of an oscilloscope, logic analyser and a waveform generator in an aluminium case measuring 110.0 x 64.0 x 24.2mm and weighing 158 grams. The software provides the user interface and functionality, and can be downloaded from the SmartScope web site. It is available for Android (Google Play Store or LabNation website), Apple Mac OS X, Apple iOS (jailbroken), Microsoft Windows 7, 8 and 10, and Ubuntu and Debian Linux distributions.

The oscilloscope provides two analogue channels with a sample rate up to 100 Msample/sec that provides a -3dB bandwidth of 30 MHz. Input signal range is ±35V with a 1 MΩ / 1 pF impedance and has an 8-bit precision and a maximal resolution of 2.5 mV.

The logic analyser offers 8 input channels with a user selectable logic level of 3.3 or 5 VDC. The SmartScope application includes a number of standard protocol decoders such as for I²C and SPI in addition to allowing custom decoders to be created. The single channel waveform generator can create arbitrary waveforms with a data rate up to 50 Msample/sec and an output level from 0 to 3.3 V. The small form-factor unit is supplied complete with a mini 'B' USB cable, 2 analogue probes, digital cable and probes for €229.

Complete article, here ▶

Magnetic-feedback ICs generate aux/standby supplies to 35W

Power Integrations' 725V InnoSwitch-EP off-line, CV/CC flyback switching ICs are aimed at "embedded" power supplies in the 20W (up to 35W) range, offering high efficiency across the load range, to meet challenging ENERGY STAR and ErP TEC requirements.

PI first used the InnoSwitch configuration in a product released in 2014. It addresses the issue of building small off-line power supplies that are long-term reliable (free from optocoupler degradation), while being accurate (using feedback and secondary-side control), and at the same time economical (without the need for a custom transformer).

The design builds, in a single IC package, the offline switching FET, primary and secondary control ICs, secondary FET drivers – and the feedback path ('FluxLink'). This is implemented as a magnetic coupling in which the leadframe is used as a single-turn winding, coupled to a further inductive loop that completes the "transformer". An adjacent anti-phase loop produces common-mode rejection of external magnetic fields and PI claims the overall design has high noise-immunity, seen as essential as the devices are aimed at markets such as white goods and appliances and may be mounted

close to motors.

The secondary side of a typical PSU that will use the InnoSwitch EP ('E' for 'embedded') uses FETs as synchronous rectifiers to improve efficiency (vs. diodes). The improved accuracy of the magnetic coupling allows the use of synchronous rectification"for free", a spokesman said.

The main differentiators from the original InnoSwitch are the inclusion of the higher-voltage off-line switching FET; and the provision of multiple outputs that are well regulated individually, and one against another. Poor cross-regulation between multiple outputs is a problem with primary-side regulation, PI asserts.

InnoSwitch-EP ICs enable 20 W power supplies to achieve approximately 90% efficiency in a multi-output design, while minimising no-load consumption to less than 30 mW. Line over-voltage regulation is highly accurate at ±5%, while ±5% OCP regulation is also achieved.

Complete article, here ▶

power is 7 µW/MHz with a 90 nm process (DCD's IP Cores are synthesisable and foundry independent). It comes with a C compiler and integrated CPU configurator, allowing it to be optimised for either ultra-low energy or for power-user projects.

D32PRO is, says DCD, a completely new, RISC 32-bit CPU that is fully scalable, "It can be easily adjusted to get the efficiency comparable to ARM Cortex M0-M3," explains Tomek Krzyzak, DCD's vice-president, "but there's no problem to run the Core with maximal performance to get up to 1.48 / 2.67 DMIPS/MHz and 2.41 CoreMarks/MHz."

DCD has released over 70 different architectures, including DQ80251 which it positions as the world's fastest 8051 CPU. Krzyzak continues, "It's a completely new, innovative solution.... why waste silicon, why limit performance, why shorten [the] peripherals list? The D32PRO answers all these questions."

The D32PRO has been equipped with Floating Point Coprocessor and a variety of available periph-

erals such as USB, Ethernet, I²C, SPI, UART, CAN, LIN, RTC, HDLC, and Smart Card. Other peripherals can be added to the CPU by using standardised interfaces.

The D32PRO emphasises low energy with a special PMU (Power Management Unit), which dynamically controls the clock's frequency. An engineer can program energy-saving mode for the CPU, where all the peripherals will be working with nominal clock. Similar to DCD's 8051 IP Cores, it is delivered with a built-in hardware debugger, tailored for the 32-bit CPU, that enables full control from Eclipse level.

Complete article, here ▶

Scalable, royalty-free 32-bit CPU IP core for deeply-embedded designs

IP Core provider and System-on-Chip design house Digital Core Design (Bytom, Poland) has its D32PRO CPU, a 32-bit, deeply embedded and royalty-free IP Core. Based on a RISC architec-

ture it boosts performance to 1.48 / 2.67 DMIPS/MHz and 2.41 Core-Marks/MHz.

The minimal usable D32PRO CPU starts from 6.8k to 10.6k gates when optimised for area: dynamic

Microchip simplifies a ubiquitous temperature measurement

Presenting it as the first integrated thermocouple electromotive force-to-degrees Celsius (emf/°C) converter, Microchip says its latest sensor-signal-conditioning IC saves design effort, space and cost. The device is the first converter IC to integrate precision instrumentation, temperature

Thermocouple Conditioning Integrated Circuit
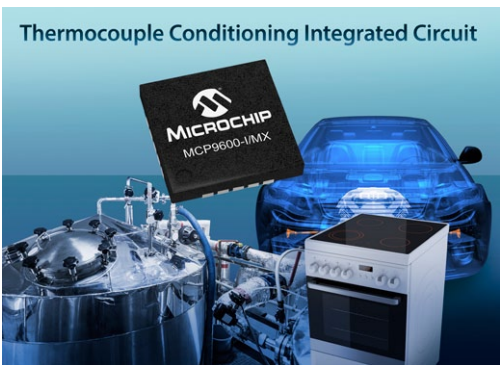
sensor and high-resolution ADC with a maths engine, to support most thermocouple types, and is the first plug-and-play solution for creating thermocouple-based designs. It removes the need for thermal design expertise or the creation of precision instrumentation circuitry, and a digital filter

minimises the effects of temperature fluctuations, system noise and EMI.

MCP9600's maths engine is pre-programmed with the firmware to support a broad range of standard thermocouple types: K, J, T, N, S, E, B and R. Thermocouples are one of the most ubiquitous temperature-measurement devices, due to their robustness and accuracy in harsh, high-temperature environments, and their ability to measure temperature over an extremely wide range. Designers do not have to create precision instrumentation circuitry to accurately measure a thermocouple's micro-volt-level signals, nor do they have to design ADC circuitry for precise temperature calculations. With the MCP9600's integrated cold-junction compensation, calculating the "Hot" junction temperature of a thermocouple does not necessitate thermal design expertise to precisely measure the reference temperature of the thermocouple's

"Cold" junction.
Other features of the MCP9600 include a temperature-data digital filter, which minimises the effects of temperature fluctuations, system noise and electromagnetic interference.

RS adds electrical design tool to free CAD portfolio

DesignSpark Electrical is the latest free software package to be made available by distributor RS Components. The tool brings time-saving and error-reduction benefits to electrical system design, RS says.

In electrical design, there are many engineers who have not had the productivity gains taken for granted in, for example, the PCB design sector – RS asserts. Perhaps the majority of engineers still work with paper design, or very general-purpose drawing/planning software. DesignSpark Electrical is a fully specified electrical CAD package with key benefits, to deliver time saving and error avoidance, for control panel, machinery and electrical system design. Among other benefits, it offers a

wiring-based approach – wiring line diagrams – to system planning that is familiar to electronic and PCB engineers.

From a connectivity base, engineers can call real components from a library, complete connectivity with automatic wire numbering (maintained through changes), and proceed to populate cabinets, with assistance in making the optimum choice in terms of cabinet size and similar parameters.

DesignSpark Electrical joins the
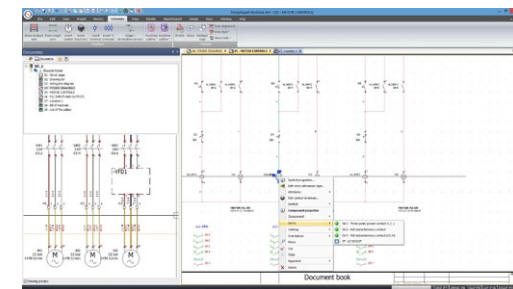
suite of DesignSpark engineering resources and continues RS' intention of removing the barriers to innovation for every engineer. As with, for example, its 3D CAD software, RS has sourced the code from a specialist in the field, in this case Trace Software which maintains a full-feature software offering in a similar space. DesignSpark 3D was written by SpaceClaim. The electrical product has been two years in development and has undergone several rounds of trials in the field. A key element of the DesignSpark

Electrical software is the integration of a library that comprises more than 250,000 components and parts, including 80,000 from Schneider Electric and 10,000 from RS, which can be added to customer designs. Other key features of the highly intuitive and highly functional software include intelligent and specialist electrical design tools, real-time referencing and validity checking to allow the creation of accurate 2D panel layouts, all of which saves time and reduces errors.

Complete article, here ▶

Knowm's memristors alive & shipping

Michael Dunn, EDN

The name memristor is formed from memory + resistor. The fundamental component it labels behaves like a resistor, but one whose value changes based on the integral of the current passing through it, hence, the memory aspect.
Innovative company Knowm is making parts and services available, with a strong focus on machine learning. It offers a package – and evaluation chip – that contains eight Memristors. As shown in the graphic, in response to successive bidirectional applied voltage "write" pulses (black), the Memristor current (red) changes value progressively; the response is essentially symmetric in both

(polarity) directions. Its behaviour as a hysteresis loop is shown in the second diagram.
The company says it is the first to develop and make commercially-available memristors with "bi-directional incremental learning" capability. The device was developed through research from Boise State University's Dr. Kris Campbell. This has been previously believed to be impossible in filamentary devices by Knowm's competitors despite significant investment in materials, research and development. Knowm claims the first commercial memristors that can adjust resistance in incremental steps in both direction rather than only one direction with an all-or-nothing 'erase'. This advancement opens the gateway to extremely efficient and powerful machine learning and artificial intelligence applications.
"Having commercially-available memristors with bi-directional voltage-dependent incremental capability is a huge step forward for
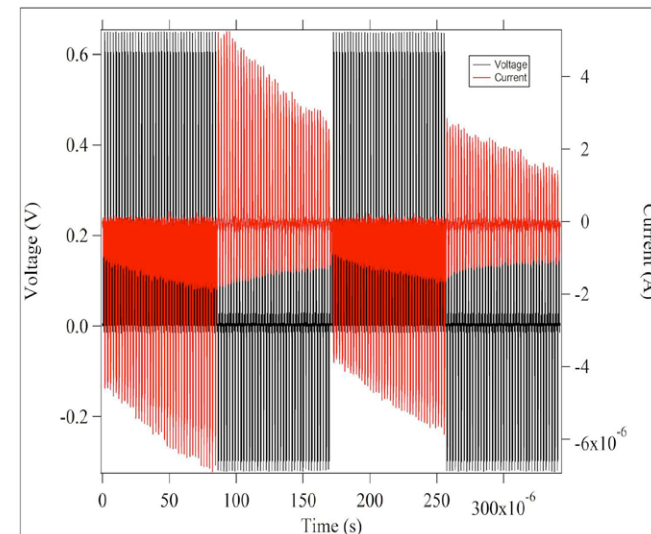
the field of machine learning and, particularly, AhaH ["Anti-Hebbian and Hebbian", see Knowm's explanation here] Computing," said Alex Nugent, CEO and co-founder of Knowm. "We have been dreaming about this device and developing the theory for how to apply them to best maximize their potential for more than a decade, but the lack of capability confirmation had been holding us back. This data is truly a monumental technical milestone and it will serve as a springboard to catapult Knowm and AHaH Computing forward."

Complete article, here ▶

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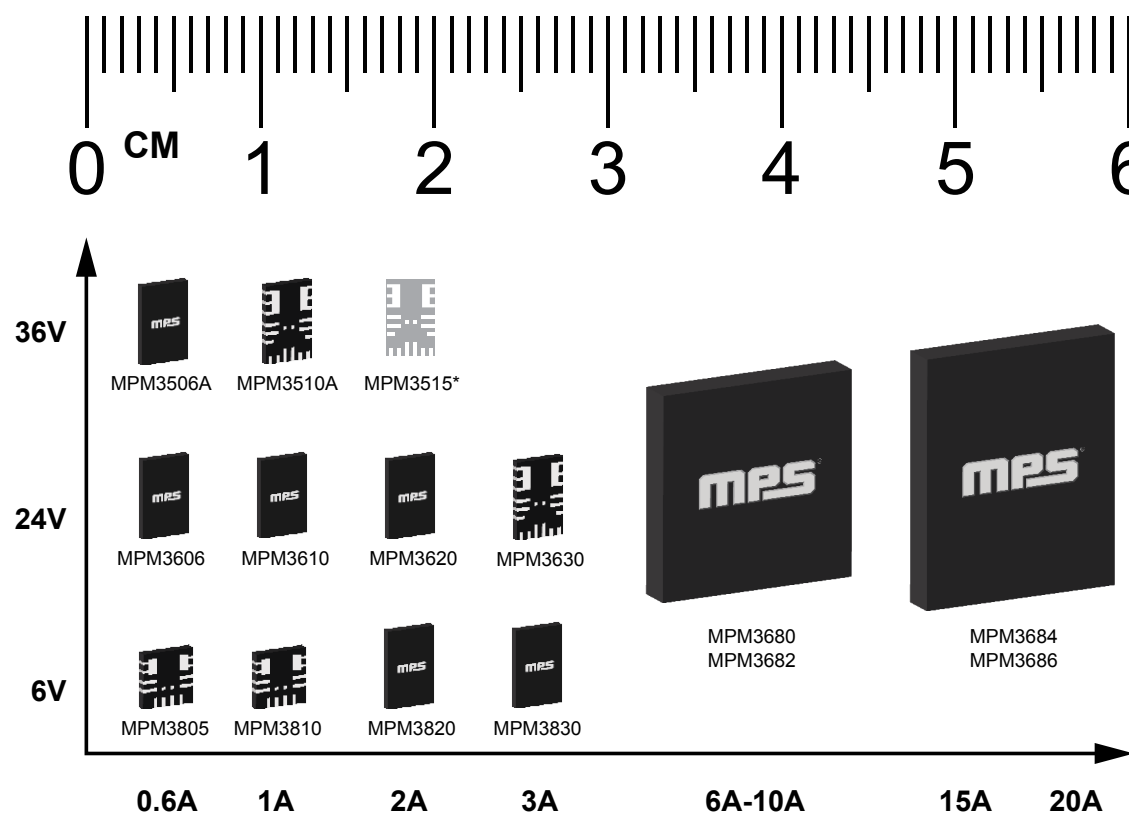
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Plug-in touchscreen makes a Raspberry Pi tablet

Distributor element14 has a 7-in. Touchscreen Display for the Raspberry Pi, expanding the ecosystem of accessories, to enable users to create all-in-one integrated projects such as turning their Pi into a tablet, infotainment system or embedded project. Compatible with Raspberry Pi 2, and Raspberry Pi 1 models B+ and A+*, the screen can be used to make 'Internet of Things' (IoT) devices with a visual display. Connect the Raspberry Pi, develop a Python script, and create home automation devices with touchscreen capability. A range of educational software and programs available on the Raspberry Pi will be touch enabled, making learning and programming easier.

Designed by the Raspberry Pi Foundation, the 800 × 480 display connects to the Raspberry Pi's DSI display connector via an adapter board that handles power and signal conversion. Touchscreen drivers with support for 10-finger touch and an on-screen keyboard will be integrated into the latest Raspbian OS for full functionality without the need for a physical keyboard or mouse.
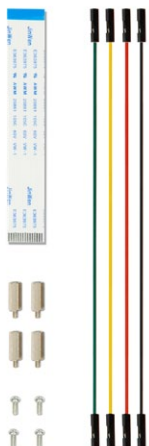
The screen dimensions are 194 x 110 x 20 mm (including standoffs), with a viewable screen size of 155 x 86 mm and screen resolution of 800 x 480 pixels.

Complete article, here ▶

650V, 100A GaN transistors on show

GaN Systems (Ottawa, Canada) displayed its GS66540C 650V 100A high current GaN power transistors for the first time at the 17th Conference on Power Electronics and Applications, EPE'15 - ECCE Europe, in September. The GS66540C (the picture is of a prior, lower-current part in similar packaging) is part of the company's family of 650V gallium nitride power transistors based on its proprietary Island Technology. These high density devices achieve extremely efficient power conversion with fast switching rates of >100 V/ nsec and ultra-low thermal losses. The GS66540C is supplied in an evolved form of GaNPX packaging specially developed for higher operating currents, providing lower inductance and greater surface mount mechanical robustness required by power modules for the industrial and automotive markets. The near-chipscale parts have no wirebonds and offer step-change improvements in switching and conduction performance over traditional silicon MOSFETs and IGBTs. Parts are, the company says, being designed in to solar, industrial and automotive applications as global manufacturers race to use the power of GaN to secure competitive advantage.

Complete article, here ▶

50 GHz hand-held combination analyser, from Keysight

Keysight Technologies has added six millimeter-wave models to its family of FieldFox

handheld analysers, including what the company claims is the first handheld combination analyser to provide coverage to 50 GHz. With more built-in capabilities than similar analysers, FieldFox can replace three or four single-function instruments — benchtop or handheld — that are typically used for maintenance and trouble-shooting of systems that operate at or above Ka-band frequencies.

"At only 3.2 kg, [these] FieldFox models deliver laboratory-grade measurements that enable field personnel to fully character-ise today's most demanding radar and satellite systems," said Dan Dunn, general manager for RF and micro-wave handheld analysers. "...a FieldFox combination analyser provides unprec-edented functionality and value at about half the cost of each equivalent benchtop instrument."

Three combination-analyser models cover 32, 44 or 50 GHz and provide spectrum analysis, vector network analysis and cable and antenna testing in a rugged, portable unit. The three spectrum analyzer models cover the same frequency range. In all six new models, spectrum measurements are up to eight times faster than those made with comparable analy-sers.

Complete article, here ▶

Evaluation boards for 5 Gbps USB 3.0-to-FIFO bridge ICs

To support design-in of its next-generation USB interfac-ing technology, FTDI Chip has a family of evaluation/development modules. Development with the company's FT600/1Q USB 3.0 SuperSpeed ICs is enabled by the UMFT60XX offering; HSMC & FMC connectivity options aid deployment into FPGA-based designs. This module family from FTDI chip (Glasgow, Scotland) comprises four models, which provide different FIFO bus inter-faces and data bit widths. Through these modules operational param-eters of FT600/1Q devices can be fully assessed and interfacing with external hardware undertaken, such as FPGA platforms from the industry's leading suppliers. UMFT600A and UMFT601A each have a high speed mezzanine card (HSMC) interface with 16-bit and 32-bit wide FIFO buses respectively. The UMFT600X and UMFT601X have dimensions of 70 x 60 mm and incorporate field-

programmable mezzanine card (FMC) connectors, again with 16-bit and 32-bit wide FIFO buses respectively. The HSMC interface is compatible with most Altera FPGA reference design boards, while the FMC connector delivers the same functionality in relation to Xilinx boards.

Fully compatible with USB 3.0 SuperSpeed (5 Gbits/sec), USB 2.0 High Speed (480 Mbits/sec) and USB 2.0 Full Speed (12 Mbits/sec) data transfer, the UMFT60xx modules support two parallel slave FIFO bus protocols with an achievable data burst rate of around 400 Mbytes/sec.

Complete article, here ▶

Simulate real-time systems behaviour – at the requirements level

Stimulus, from Argosim, is a software tool for simulating and validating systems descrip-

tions at the requirements stage, allowing them to be expressed in a form close to natural language, that nevertheless has precision and rigour.
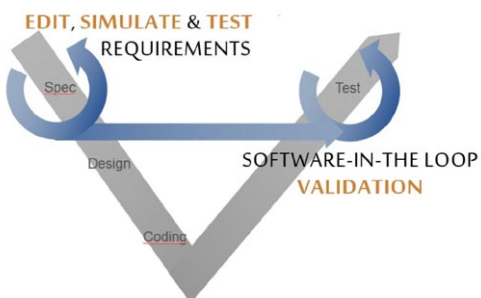
Argosim contends that 40 to 60% of design bugs are caused by faulty design requirements: that is, inherent flaws in designs even before they are coded, compiled or any of the other downstream processes leading to an executable. The aim is to, "address the challenge of verifying system requirements at the specification stage—before design begins."

Using the Stimulus product, you might begin with a requirements document in plain text. Argosim makes the point that there are numerous tools that relate to requirements traceability, or requirements management; but that Stimulus is concerned with validation. From the plain text, the user re-creates the description in a form that is still immediately readable, but is formed around a library of key words or operators, instantiated by a drag-and-drop process. Example terms are English words such as "when", "then", "initially" and "afterwards". These retain their intuitive plain-language meaning (or very close to it) but when selected from the library, are underpinned by a rigorous, formal-methods-derived meaning, as interpreted by the Stimulus tool. The user adds parameter values that – critically – can be time-related. Stimulus can then simulate the behaviour of the system, revealing how the formally-expressed sys-

tem will perform vs. the requirements. In its specification phase, Stimulus therefore supports definition of requirements; of generic test requirements; and simulation of the requirements – all leading to validation of the requirements. In a second, testing phase, the tool will generate test vectors from generic test requirements, and will verify that the system is consistent with the text-based specification. The

test vectors can be carried forward for use in a test bench in the later phases of the project. Inputs to the simulation process can be randomly-defined over the range of possible values that the system will experience. The tool, as a company spokesman expresses it, "maps the constrained space of system behaviour."

Complete article, here ▶

80A from a digital power integrated PoL module

Intersil claims a first for its encapsulated 80A digital power module, the ISL8273M, that the company designed as a high power density POL (point of load) solution for advanced FPGAs, processors and memory. ISL8273M is a complete step-down regulated power supply that delivers up to 80A output current and operates from industry standard 5V or 12V input power rails. Multi-phase current sharing of up to four ISL8273M power modules enables

power supply designers to create a 320A solution with output voltages as low as 0.6V. In an 18 x 23 mm module, the ISL8273M is aimed at space-constrained data centre equipment and wireless communications infrastructure systems.

Claiming twice the output current of comparable digital power modules, the device's High Density Array (HDA) package offers a high level of electrical and thermal performance through a single-layer

conductive package substrate that reduces lead inductance and dissipates heat primarily through the system board. Through a PMBus-compliant interface, the module's digital control technology provides precise sequencing, full telemetry and system monitoring. The ISL8273M can also start up and operate in pin-strap mode

using six external resistors for setting default configurations such as Vout, soft-start, under-voltage, switching frequency and current sharing. This allows designers to power up the modules during the development phase without using PMBus or requiring any programming.

Complete article, here ▶

Tensilica DSP core targets 4k mobile imaging

From Cadence's Tensilica IP operation, the Vision P5 digital signal processor is intended to enable 4k imaging on mobile devices, with claimed metrics of 13x increase in performance and a five-fold reduction in energy (for the imaging function). The core will, Cadence says, offload its host CPU to minimise energy consumption, and will seek applications in image and video enhancement, stereo and 3D imaging, depth map processing, robotic vision, face detection and authentication, augmented reality, object tracking, object avoidance and advanced noise reduction.

The Tensilica Vision P5 has been specifically configured for applications requiring ultra-high memory and operation parallelism to support complex vision processing at high resolution and high frame rates, Cadence adds, off-loading vision and imaging functions from the main CPU to increase throughput and reduce power.

The core includes an expanded and optimised Instruction Set Architecture (ISA) targeting mobile, automotive advanced driver assistance systems (or ADAS, which includes pedestrian detection, traffic sign recognition, lane tracking, adaptive cruise control, and accident avoidance) and Internet of Things (IoT) vision systems. Cadence also says that the design has improved the ease of software development and porting, with support for integer, fixed-point and floating-point data types and an advanced toolchain with an auto-vectorising C compiler. The software environment also features complete support of standard OpenCV and OpenVX libraries for fast, high-level migration of existing imaging/vision applications with over 800 library functions.

Complete article, here ▶

CONTINUOUS TIME SIGMA DELTA ADCS

BY IAN BEAVERS, ANALOG DEVICES

Pipeline ADCs are Nyquist-rate discrete time architectures that will have flat quantisation noise from DC to the Nyquist frequency. Alternate ADC architectures can be implemented for applications not requiring a full Nyquist bandwidth.

Band-Pass continuous time sigma delta (CTΣΔ or CTSD) ADCs use a noise shaping function that essentially 'pushes' or filters the in-band quantisation noise outside of the frequency band of interest. In comparison to a discrete time ADC, a CTSD does not use a switched capacitor to sample the input signal.

The noise of a CTSD ADC will be shaped based upon the loop filter response within the modulator. This causes the noise transfer function to have a non-flat shape that is notched considerably lower over a narrow band of interest. It is in this band that the CTSD ADC operates to its maximum perfor-

mance where the SNRFS is the highest. The AD6676 is a new CTSD IF receiver subsystem with noise spectral density as low as -159 dBFS/Hz across a 20-160 MHz tunable frequency band.

Since one of the main benefits of a CTSD architecture is to detect signals within a narrow frequency band, operation across the wide sampling band is not of particular interest. Instead, the dynamic range within the narrow pass band is what will be highlighted as the performance metric for a CTSD ADC.

Main highlights:

- Oversampling provides inherent anti-aliasing as harmonics fall out of band beyond the BW of the CTSD. Distortion products would need high frequency components well beyond Fs/2 in order to alias back within the pass-band.
- CTSD architectures use resistive inputs that are easier to drive
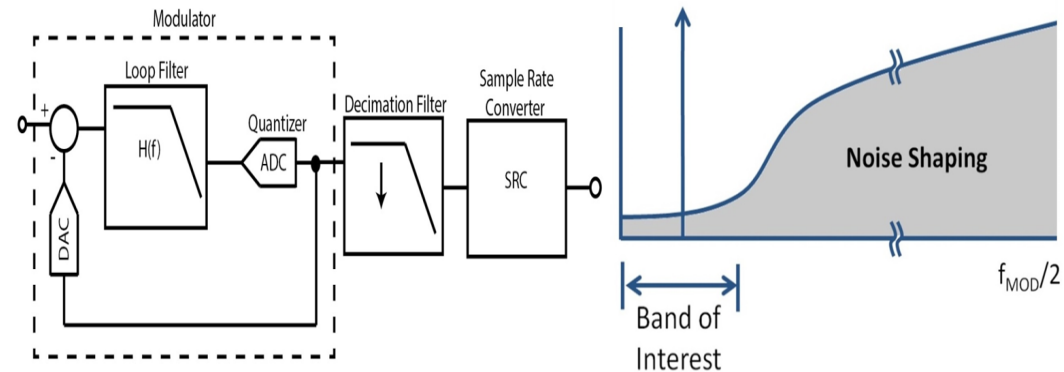
Figure 1. *CTSD architectures are based upon loop and decimation filters that shape output noise.*

compared to switched capacitor inputs.
- The requirements for band specific IF anti-aliasing filters can be significantly relaxed due to the pass-band benefits of the internal loop filter, simplifying system architecture.

Some drawbacks:

- A very high frequency clock is needed to achieve an effective oversampling ratio (OSR). For example, a 100 MHz BW CTSD with an OSR of 16 requires a

sampling clock of;
$Fs = 2*100\ MHz*16 = 3.2\ GHz$.
- Programmable attenuation prevents an over-range condition that can temporarily create unstable operation in the feedback loop.
- Decimation filtering is needed to provide the narrow band of interest at the output of the CTSD using post digital processing. Quadrature down conversion and additional selectable decimation for a tunable frequency band are additional features.

EMBEDDED SYSTEMS

USART VS UART: KNOW THE DIFFERENCE   BY JACOB BENINGO

Have you ever used the term UART only to be corrected by another engineer that it isn't a UART but USART? In certain circumstances the interchangeability of these terms may be appropriate but in many cases it is in error. Let's examine what a USART and a UART are, and discuss the major differences.

Most embedded engineers are familiar with a UART: a Universal Asynchronous Receiver/Transmitter. It is a microcontroller peripheral that converts incoming and outgoing bytes of data into a serial bit stream. A start bit initiates the serial bit stream and a stop bit (or two) completes the data word. A UART also has the option of adding a parity bit to the stream to assist in detecting if a bit error occurs dur-ing transmission. Figure 1 shows a standard example of what an engineer would expect to see from data transmitted through a UART.

A USART -- a Universal Synchronous/Asynchronous Receiver/Transmitter -- is a microcontroller peripheral that converts incoming and outgoing bytes of data into a serial bit stream. Hmm. The definition of a USART is identical to that of a UART, but with "synchronous" added to the term. Surely there are some more meaningful differences? Otherwise, a USART would just be known as a UART.

Well, there are differences – important ones. The first difference between a USART and a UART is the way in which the serial data may be clocked. A UART generates its data clock internally to the microcontroller and synchronises that clock with the data stream by using the start bit transition. There is no incoming clock signal that is associated with the data, so in order to properly receive the data stream the receiver needs to know ahead of time what the baud rate should be.

A USART, on the other hand, can be set up to run in synchronous mode. In this mode the sending peripheral will generate a clock that the receiving peripheral can recover from the data stream without knowing the baud rate ahead of time. Alternatively, the link will use a completely separate line to carry the clock signal. The use of the external clock allows the data rate of the USART to be much higher than that of a standard UART, reaching up to rates of 4 Mbps.

The second major difference between a USART and a UART is the number of protocols the peripheral can support. A UART is simple and only offers a few options from its base format, such as number of stop bits and even or odd parity. A USART is more complex and can generate data in a form corresponding to many different standard protocols such as IrDA, LIN, Smart Card, Driver Enable for RS-485 interfaces, and Modbus, to name a few. A USART also has the same asynchronous capabilities as a UART, that is, a USART can generate the same type of serial data as seen in Figure 1.

USART and UART peripherals have definitely different capabilities and can be useful in different situations, so a developer may find
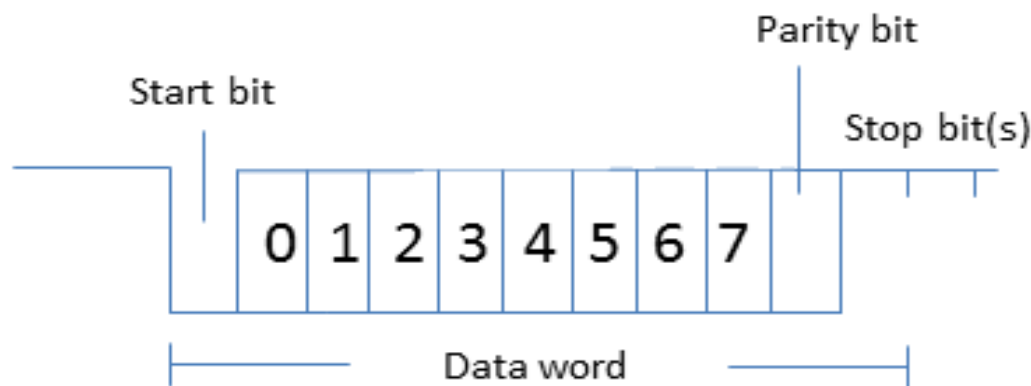

Figure 1 *UART serial data*

both peripherals onboard a standard micro-controller. For example, take a microcontroller that is targeting low-power design such as the STM32 family. The STM32 parts have both a USART and a UART peripheral on-chip. The USART is meant to do all of the "heavy lifting" serial communication during periods of "high" energy consumption. When the microcontroller is asleep and in a low power mode, though, the UART peripheral can handle low speed communications while offering a reduced energy footprint.

Are USARTs and UARTs the same? Technically the answer is no. A USART generally has more capabilities that a standard UART and the ability to generate clocked data allows the USART to operate at baud rates well beyond a UART's capabilities. A USART does encompass the capabilities of a UART, though, and in many applications, despite having the power of a USART, developers use them as simple UARTs, ignoring or avoiding the synchronous clock generation capability of these powerful peripherals. No wonder so many people use the terms as though they were synonyms.

Jacob Beningo is a Certified Software Development Professional (CSDP) whose expertise is in embedded software. Feel free to contact him at jacob@beningo.com, at his website www.beningo.com, and sign-up for his monthly Embedded Bytes Newsletter here.

DVCON EUROPE 2015 ANNOUNCES TECHNICAL PROGRAM

The Design and Verification Conference (DVCon) and Exhibition Europe (Munich, 11th & 12th November 2015) takes as its scope. "the application of languages, tools and intellectual property for the design and verification of electronic systems and integrated circuits."

Sponsored by Accellera Systems Initiative, DVCon Europe brings chip architects, design and verification engineers, and IP integrators the latest methodologies, techniques, applications and demonstrations for the practical use of EDA solutions for electronic design.

The content in the Technical program for this year's event has now been published. Chairman of the Steering Committee, Martin Barnasconi (NXP Semiconductors) set the objective of addressing design and verification across the product design value chain; his aim in compiling the program has been to attract, and provide information for, engineers working across a broad spread of companies, and in many different roles within those companies.

That said, he identifies a number of key themes that have informed the 2015 program;

in the Automotive arena, issues of safety and security; the trend towards self-driving vehicles, and their functional safety. In the Semiconductor space, the program has a focus on another sector that is strong in Europe – mixed-signal IC design. It has long been the case that design and verification in this space has been more fragmented than in the logic domain, and a theme of the Conference program is how AMS (analogue/mixed-signal) design and verification can be made more coherent. Added to that is the general trend to low power in all forms of design.

Barnasconi notes that in the first running of DVCon Europe, the training content was a well-received component; accordingly, there will be extensive tutorial and seminar content, as well as conference papers; plus the opportunity for verification professionals to meet and, "look over the fence" at what others are doing.

The initial announcement of the DVCon Europe 2015 program was covered here; and a longer account of the Technical Program content, and the approach that went into it, is here.

SAVE POWER IN IOT SOCS BY LEVERAGING ADC CHARACTERISTICS

By Manuel Mota, Synopsys -August 21, 2015

Power-sensitive applications such as Internet-of-Things (IoT) require a comprehensive power savings strategy within the system-on-chip (SoC). Techniques relying solely on the use of traditional power-down modes and low supply voltage may not be enough to achieve the required power targets. The analogue block is often assumed to be too sensitive and not compatible with aggressive power management techniques.

However, a good understanding of the analogue block's characteristics can enable low-power SoC designs. In this article we take a closer look at the analogue-to-digital converter (ADC) IP interfacing with external sensors in a general purpose IoT SoC design and describe its relevant characteristics that can be exploited at the system level to achieve low-power consumption.

Challenges of traditional low-power techniques

IoT applications, possibly operating on coin-cell batteries or energy harvesting, are driving the requirements for very low-power consumption SoC designs across the industry. In order to sustain operation for a long period of time

without replacing the batteries, designers must make the most of the available power reduction techniques.

The traditional approach relies on reduction of the SoC's supply voltages and on the finer geometry process' smaller feature size to

reduce active power. This approach increases system costs and potentially leads to higher leakage power.

At the system level, it is possible to implement low-power techniques by identifying blocks in the chip that can be powered down when certain actions are being performed. It is also possible to adjust the clock rate and supply level to the minimum that sustains the performance of the required actions, thus sav-
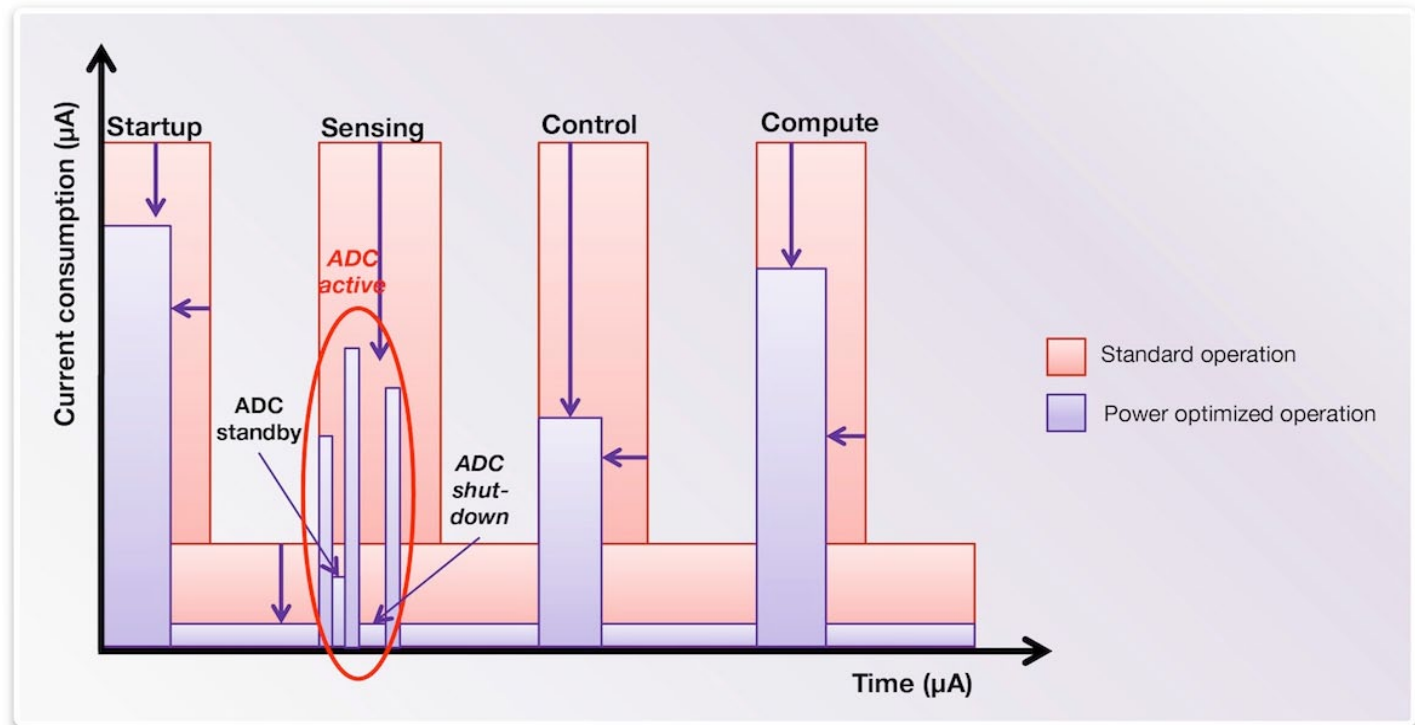

Figure 1. *Common IoT usage profile*

ing additional power.

An IoT SoC's typical activity profile is characterised by its very short duty cycle: most of the circuit is often in idle mode; only a small portion of the circuit is intended to be always active in order to scan the environment and activate the remaining circuitry when needed. (Figure 1). The always-active circuitry is placed on a dedicated power island and uses high Vth (threshold voltage) devices or even thick oxide devices to minimise leakage power. The remaining circuitry can be switched off from the power supply to limit its leakage.

A voice-activated appliance is an example of such application, where only the simple voice detection circuitry is active all the time, and the blocks dedicated to command recognition and processing are activated only when the voice detection circuit identifies a potential command. Another example is the regular poling of sensors to determine if some change in the environment requires action to be taken.

Therefore, modern IoT SoC designs implement complex power management architectures with multiple power-down modes and detailed partitioning of the circuit into separate power islands in order to further reduce active and leakage power consumption.

However, when it comes to analogue interfaces, traditional low-power techniques cannot be applied directly. Analogue blocks are typically required to handle signals with a large voltage swing and high linearity requirements. This limits the ability to reduce power supply levels and thus the effective minimum feature size.

Analogue blocks have internal biasing currents and voltages that need to settle properly for best performance, therefore power up and power down times are inherently slow, limiting the ability to change power modes to where the interface may not be in use for extended periods of time. Additionally, they are sometimes accessed by external devices that are controlled via slow serial busses, which results in a limited ability to actively control their power state in real time.

Designers need a new approach to overcome such limitations, particularly when designing power-sensitive applications. Integration of ADCs that interface with the sensor not only reduces external bill-of-materials (BOM) cost but also enables a tighter integration of the analogue interface into the SoC's power management architecture, enabling faster power up and power down transitions and additional power savings. To reduce BoM cost and power dissipation, designers must select an integrated ADC that is flexible enough to support the different modes of operation with minimal power dissipation and can change quickly between different power modes. The key features of an integrated ADC are:

- Minimal static power dissipation, resulting in minimisation of the power consumption as speed is reduced
- Several performance modes, where power is minimised as performance settings are reduced
- Multiple power modes, with the ability to change between them quickly and without losing accuracy/performance

Specific use cases

Designers must understand all the features of the ADC and how they can be used in specific use cases to achieve additional power savings.

The author continues by outlining examples of several use cases, that provide examples of where low-power techniques can refine today's system-on-silicon designs for the Internet of Things. Click for pdf.

MULTITOUCH ARRIVES FOR LARGE DISPLAYS

BY CHARLES LIMONARD, DIALOG SEMICONDUCTOR

Multitouch interfaces have revolutionised user interfaces to computers but we have only just begun to see what they can do in applications that have previously had access only to simple touch interfaces or are just beginning to become digitised. This is particularly true of applications that call for touch interaction on larger display panels.

Signs and billboards based on multitouch technology can provide new ways for advertisers to interact with potential customers, allowing them to spin and zoom in on products displayed in an end-of-aisle display within a shop or a large panel outdoors. In schools and colleges, teachers and students can move from simple electronic whiteboards to interactive displays that let them find images and text online and then zoom in annotate them for the rest of the class.

In industrial and other real-time control-oriented applications, multitouch makes it possible to bring more controls into the touchscreen, letting operators highlight objects on the screen to see their detailed state and then dial in new parameters instead of having to type in detailed commands or find a relevant control among the many spread across a nearby control panel.

In medicine, surgeons can rotate and zoom in on X-rays and tomographs using now familiar pinching and spreading gestures to get a better look at areas of the image that need closer inspection before making a diagnosis or accurately marking the area for surgery.

The technology could even make furniture interactive. A number of universities and companies, including Microsoft, have investigated interactive surfaces for tables that not only detect the touches from users sitting around them but objects placed on the top – a feature that makes possible augmented reality games and other forms of entertainment.

However, these applications can only come to life with the right technology. Projected capacitive touchscreen have driven the revolution in multitouch within portable electronic devices such as phones and tablets but the technology is largely unsuitable for applications beyond these. One problem is scalability to larger displays. The technology becomes less accurate as the screen size increases and it does not handle the 65in-plus displays needed for whiteboards and interactive signage.

A further problem is the nature of the touch itself. Capacitive touchscreens require that, to be registered by the sensor's electronics, the touching element have some capacitance. A naked finger or specially designed stylus satisfies this requirement but a gloved finger will probably not be detected unless the glove is very thin. The technology will also not function properly when wet, making it difficult to justify for outdoor signage as well as in medical, industrial and domestic table-top environments where liquid spills can occur easily.

In-glass multitouch technology offers an alternative that satisfies all of the requirements of these applications.

The author continues by outlining the basic principle behind the in-glass sensing technique, and expands on how it can enable an expansion of the HMI space in which touch becomes an ideal method of interaction. Click for pdf

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PROGRAMMABLE MIMO

PROGRAMMABLE RF AND OPEN-SOURCE SOFTWARE; A NEW APPROACH FOR ADVANCED WIRELESS

BY EBRAHIM BUSHEHRI, LIME MICROSYSTEMS

Radio frequency (RF) design is changing under the pressure to support faster data transfers for increasingly mobile users. This next phase in the evolution of mobile communications calls for much greater flexibility in the way that transmitters and receivers are configured. It calls for a shift away from traditional front-end RF architectures.

Today's wireless LAN and cellular protocols are already close to the theoretical limit in terms of being able to deliver data over a link for a given amount of energy. To increase the information density of networks, wireless designers need to accommodate a combination of techniques. They include greater use of spatial multiplexing through the deployment of much smaller cells in urban areas, which allows maximum reuse of RF spectrum across a service provider's area.

Multi-mode operation

Systems will need to cope with multiple frequency bands and protocols. A small-cell basestation will often need to be able to handle WiFi and 4G traffic, with other wireless protocols such as white-space radio potentially being added to support the Internet of Things.

Rapid interface deployment will be a key requirement for small-cell systems used in urban areas where it is too expensive to have individual basestations updated physically to handle changes in demand for specific protocols and usage profiles.

Interfaces may even be redeployed dynamically to cope with changes in traffic patterns. During the daytime, a more static user base may favour WiFi. At night and commute times, 3G and 4G are likely to be more appropriate protocols. They are better at accommodating the frequent hops between cells needed by a transient user base.
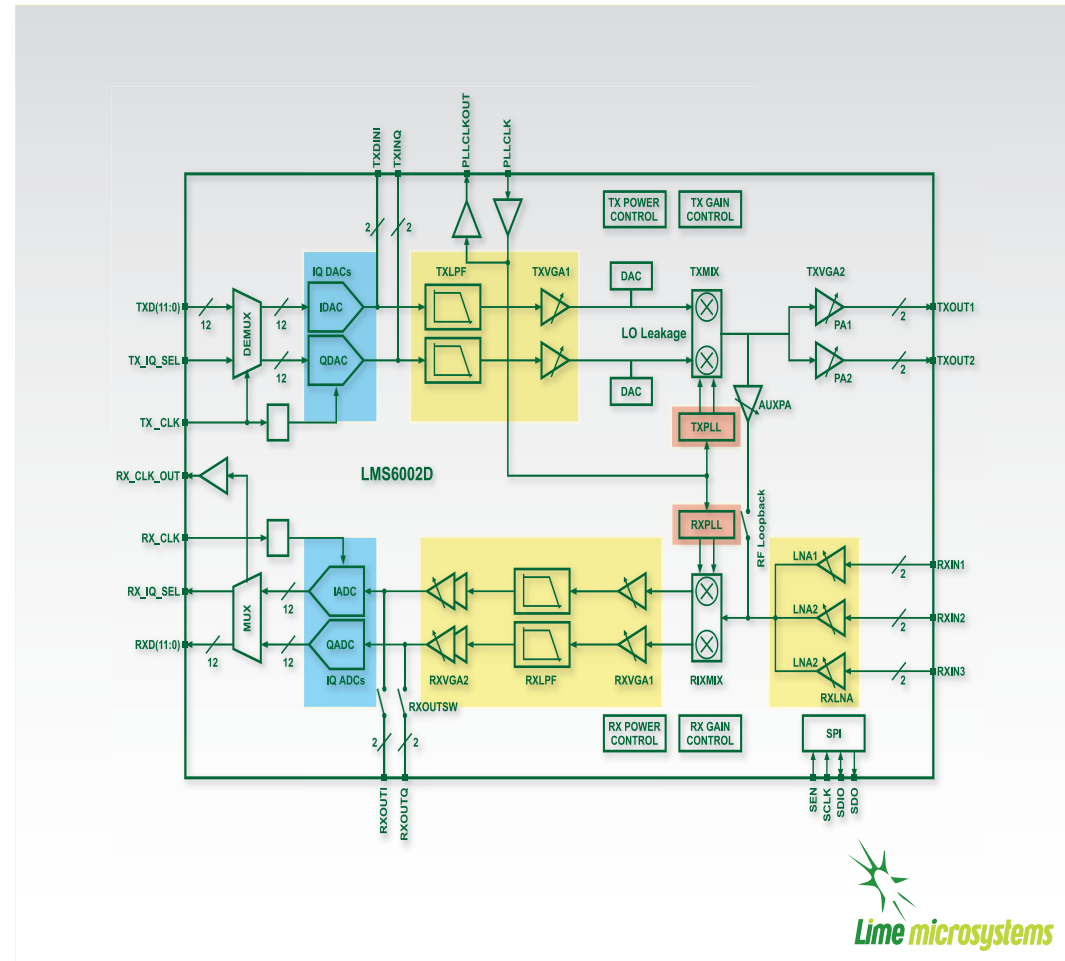

Figure 1. *The LMS6002D was Lime Microsystems' first volume IC, offering a 28 MHz bandwidth in the range 300 MHz to 3.8 GHz.*

PROGRAMMABLE MIMO

Within a given wireless standard, spatial diversity is becoming an important tool for improving signal quality and, with it, achievable datarates. Spatial diversity greatly improves the chances of a receiver being able to decode a signal that has been split and reflected many times over. By detecting the subtle differences in signal behaviour received by multiple antennas, the decoder has a much greater chance of interpreting the signal correctly. A similar technique can be used for transmission, sending subtly different signals on multiple antennas to improve the chance of a receiver decoding the signal correctly after numerous phase shifts, attenuations and other distortions.

MIMO antenna arrays

Multiple-in, multiple-out (MIMO) antenna arrays that employ a large number of elements provide opportunities to use beamforming techniques to dynamically steer signals towards fast-moving users. The use of beamforming does not just improve reception for the user; it reduces interference with other signals and increases the security of transmission. By reducing the signal power that reaches eavesdroppers, beamforming is also suited to covert communications and military requirements. The ability to dynamically configure radio interfaces allows applications that require extremely high availability to overcome interference and jamming attempts.

The drive to add antennas to improve transmitter and receiver performance puts greater pressure on product design. It calls for an architecture that represents a departure from conventional radio-system design.

A receiver in a radio system typically relies on a front-end unit that extracts channels of interest from a selective band within the radio spectrum received by a single antenna and downconverts these high-frequency signals to baseband such that they can be processed by a subsystem that performs demodulation and conversion to a digital bitstream. Transmission reverses the process, in which the modem receives a digital bitstream bearing data and creates a modulated signal that is passed to the RF subsystem for transmission over the wireless channel.

The problem that faces designers of multi-standard radios that incorporate increasingly sophisticated MIMO techniques is that conventional front-end RF designs call for the use of fixed-function hardware, often using a combination of application specific integrated circuits (ASICs) and discrete RF and analogue components to support each target air-interface standard. Although interface-specific components will often allow some flexibility, such as the choice of a narrow range of channels through software control, the flexibility is limited.

Traditional RF processing architectures have been optimised around the use of fixed-function circuitry. For example, the downconversion to baseband performed by a receiver will often employ heterodyne techniques. In the past, these were highly cost-effective to implement. But, because traditional heterodyning techniques demand the use of devices tuned to specific frequency ranges, they become increasingly onerous to implement in a multistandard environment. Each option demands a different combination of discrete components and filters, making it difficult to squeeze multiple transmit and receive channels onto a single PCB.

The article continues by considering the characteristics of today's cellular RF stages that indicates the need for a programmable future. Click for pdf.

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USING INFINITE SYNTHESIZED NETWORKS (ISN) DESIGN TECHNIQUES TO CREATE RF FILTERS

By Bob Hammond, Resonant Inc

The demand for wireless capacity to connect mobile devices and the emerging Internet of Things (IoT) to data networks is growing at an astronomical rate. Analysts forecast that there will be 11.5 billion mobile-connected devices by 2019 [1], and that by 2019, mobile data traffic will reach 25 exabytes—or 25 million gigabytes— per month, a ten-fold increase from 2014 levels. [2]

Manufacturers of connected devices are already struggling to keep up with the proliferation of spectrum bands needed to carry this data. While available space on the circuit board continues to shrink, the need to provide users with access to these bands continues to increase.

As a result, connected devices require more RF components, adding to costs and power demands. This is forcing mobile phone manufacturers to add new models just to keep up with bandwidth needs, at a time when they would actually prefer to be reducing the number of different models and SKUs (Stock-keeping units).

The proliferation of frequency bands and the desire to reduce the number of phone SKUs is putting enormous pressure on RF component and module manufacturers to reduce size and
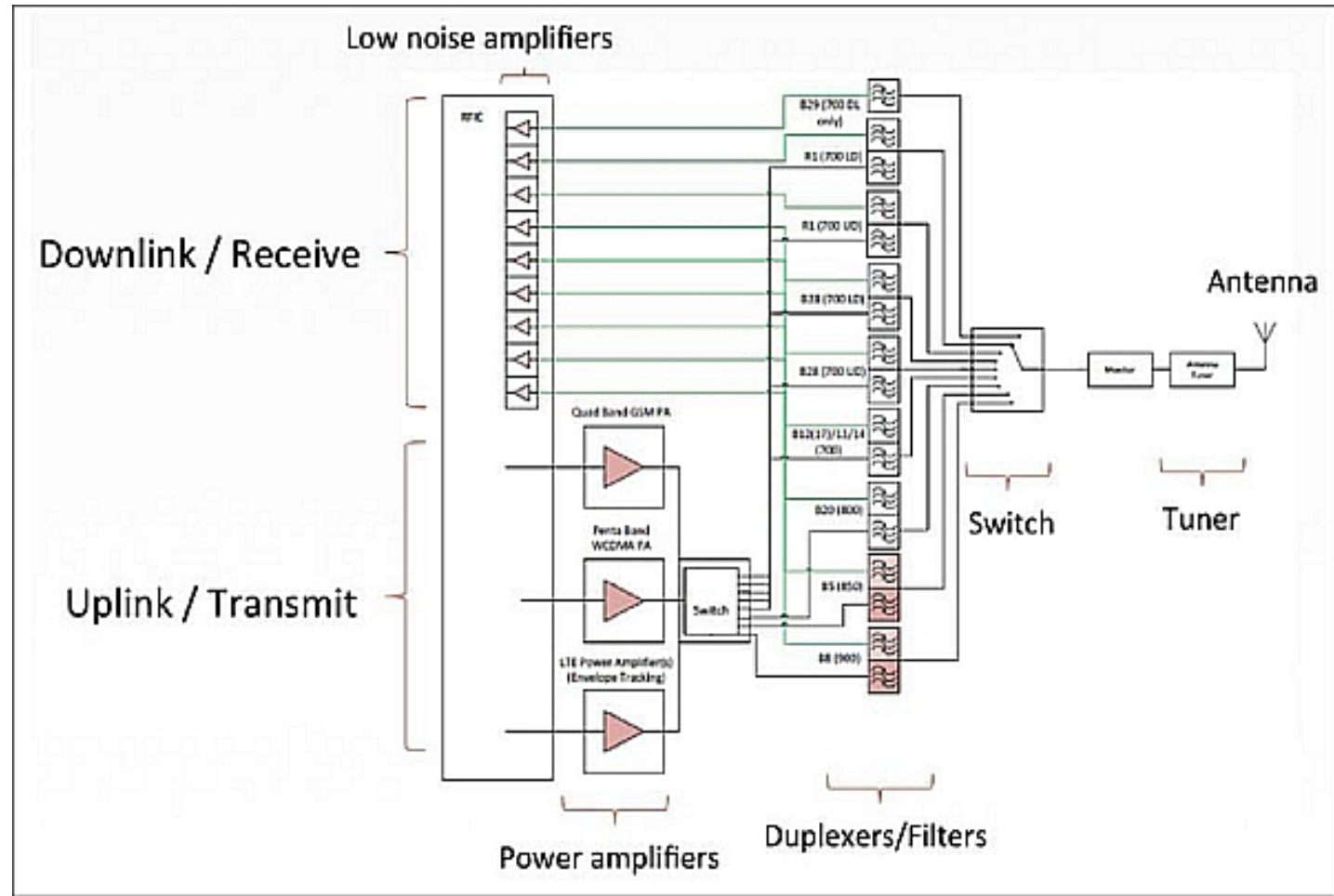

Figure 1. *RF front-end architecture for the Low-Band frequencies (700-900MHz), illustrating the complexity of the front-end.*

cost, while at the same time improving performance. Going forward, carrier aggregation and more complex Multiple-In-Multiple-Out (MIMO) designs, enabling the emerging LTE-Advanced and 5G networks, will require dramatically smaller and cheaper RF filters.

Infinite Synthesized Networks (ISN) is a new filter design technique that can be used to develop a state-of-the-art Band 3 duplexer using low-cost SAW (surface-acoustic-wave) fabrication, while achieving performance results that equal or exceed the performance of the very best available, but more costly, BAW (bulk-acoustic-waveBand 3 duplexer.

RFFE complexity
The mobile RF front-end (RFFE) is becoming increasingly complex. With more spectrum auctions scheduled for the future, leading to the adoption of LTE-Advanced with key features of carrier aggregation (CA) and multiple-in-multiple-out (MIMO) for increased data throughput, there appears to be no slowdown in this increasing complexity—or in the need to simplify the RF front-end architecture.

The current RFFE architecture comprises the following components (Figure 1):
- Antenna tuner
- Antenna switch
- Duplexers and filters
- Power amplifier switch

- Multi-mode, multi-band power amplifier (MMMB PA)
- Low noise amplifiers
- Matching networks

Power amplifiers, which in the past were the high cost component of the RFFE, have now advanced to a point where a single power amplifier can cover multiple technology modes, such as CDMA, LTE, W-CDMA and multiple frequencies/bands—hence the terms Multi-Mode/Multi-Band (MMMB) PAs. Although filters and duplexers are relatively low-cost items, a filter is required for every RF path. Thus the most significant cost for the RFFE moving forward, is the filters.

A receiver in a radio system typically relies on a front-end unit that extracts channels of interest from a selective band within the radio spectrum received by a single antenna and downconverts these high-frequency signals to baseband such that they can be processed by a subsystem that performs demodulation and conversion to a digital bitstream. Transmission reverses the process, in which the modem receives a digital bitstream bearing data and creates a modulated signal that is passed to

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The article continues by describing filter design with Infinite Synthesized Networks, a set of design tools that bring together modern filter theory, finite element modelling (both electro-magnetic and acoustic), and new optimisation algorithms. Click for pdf.

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ACHIEVING 2 GHZ ANALYSIS BANDWIDTH IN MMWAVE 5G TEST AND MEASUREMENT

MARTIN SCHMAEHLING, ROHDE & SCHWARZ

Mobile networks beyond LTE will place new requirements on test and measurement. The boom in mobile Internet access due to smartphones and tablet PCs has made LTE and LTE-Advanced the fastest growing mobile technologies.

Because of the requirements of smartphones and tablet PCs, LTE and LTE-Advanced have been optimised for high data throughput to wireless users. However, when it comes to the requirements for 2020, it is foreseen that many new scenarios and applications need to be supported. These requirements and possible solutions are a topic of 5G research. Traditionally the official definition of next-generation mobile communications systems comes from the ITU. Today, the future 5G requirements are being studied.

The Internet of Things (IoT) is a concept whereby more and more devices such as emergency systems, robots and home automation equipment will increase the number of connected devices many times over. The requirements of these devices will differ vastly from those of smartphones or PCs. Some will require extremely high data rates, while others

Figure 1 *R&S FSW signal and spectrum analyser with R&S RTO oscilloscope.*

will send or receive minimum amounts of data and require the simplest possible radio access procedure and many years of battery lifetime.

The Tactile Internet aims to support steering and control via the Internet. Examples range from mobile gaming and remote control of robots to healthcare applications. For consistent user perception, round-trip times in the order of 1 msec are required.

Today's cellular technology cannot meet these requirements. We therefore anticipate that 5G will require much wider frequency bandwidth, which is only available in the millimeter-wave realm. Bandwidths up to 2 GHz are being discussed. New waveforms and new modulation schemes are also in prospect.

Millimeter-wave bands
One area of 5G studies is to explore radio wave propagation characteristics at higher carrier fre-

quency, also referred to as channel sounding. While mobile network operators and network vendors have experience in frequencies from 700 MHz to 3 GHz for cellular networks, milli-meter-wave technology and signal propagation is a new realm.

Exploiting the required frequency bandwidths will require "mining" new frequency bands. Universities in the USA have conducted early research on the propagation characteristics of a 28 GHz signal in an urban environment. Recent investigative work by several research initiatives all over the world now includes using the 60 GHz ISM bands and frequencies around 73 GHz. A network operator in South Korea has announced that it will run a 5G network at the 2018 Winter Olympics in PyeongChang in the 28 GHz range.

New waveforms
The LTE air interface does not efficiently meet all 5G requirements. The 10 msec frame dura-tion is too long for round-trip times to meet the requirements of tactile applications. The cy-clic prefix is considered overhead and causes latency. Therefore, other means are needed to avoid intersymbol interference (ISI) and inter-carrier interference (ICI). A filtered multicarrier approach is being studied in order to achieve synchronous/asynchronous traffic types, with loss of orthogonality in some cases. Different

techniques are being investigated, such as filterbank multicarrier (FBMC), universal filtered multicarrier (UFMC) and generalised frequency division multiplexing (GFDM).

Ultrawideband signal analysis
Mobile devices require physical layer confor-mance tests in line with their specific stan-dards. The required transmission test param-eters and procedures with LTE, for example, are defined in the standards 3GPP 36.141 (for base stations) and 3GPP 36.521 (for mobile devices). These parameters and procedures include spectral measurements at frequencies up to 12.75 GHz and signal demodulation with up to 20 MHz analysis bandwidth.

Signal and spectrum analysers are used for these tests. However, because of the required frequency range and analysis bandwidth, the anticipated requirements for 5G testing cannot be met in the same straightforward way as in the case of LTE.

Combining the advantages of a spectrum analyser with the bandwidth of an oscilloscope In order to digitally demodulate signals, the spectrum analysers is the instrument of choice.

Spectrum analysers with demodulation band-width up to about 500 MHz are commercially available today.

Combining the advantages of high-end spec-trum analysers for spectral measurements with those of cost-efficient midrange oscilloscopes is a concept in signal analysis that extends the analysis bandwidth to up to 2 GHz. The analy-ser downconverts to an intermediate frequency (IF). The IF of the spectrum analyser must be high enough to support the required frequency bandwidth. In addition, it must still be low enough for the oscilloscope to fulfill the Nyquist sampling theorem. Such a combination is de-picted in Figure 1, showing an R&S FSW signal and spectrum analyser with an R&S RTO1044 oscilloscope.

This article continues by outlining how the combined resources of high-end spectrum analysers and oscilloscopes can address the new measurement challenges. Click for pdf.
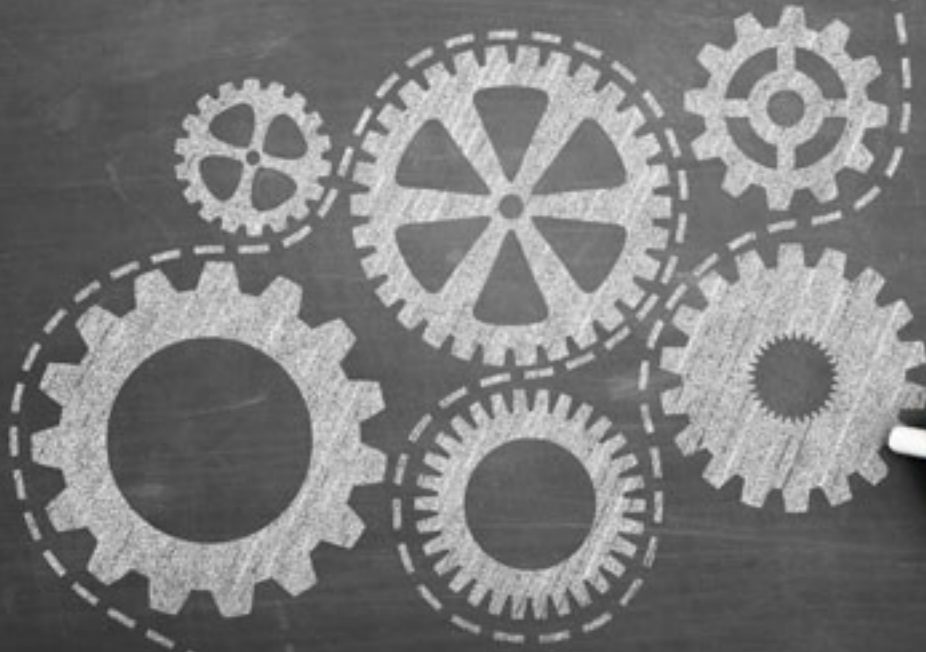
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designideas

- Single-MOSFET circuits gate & modulate
- Modded charge pump extracts power from digital signal

Single-MOSFET circuits gate & modulate   By Umar Shami

Discrete small-signal MOSFETs still find uses today, and this Design Idea presents two simple examples: an AND gate, and an amplitude modulator.

Figure 1 shows a standard two-input AND gate along with its MOSFET (and one- or two-resistor) implementation.
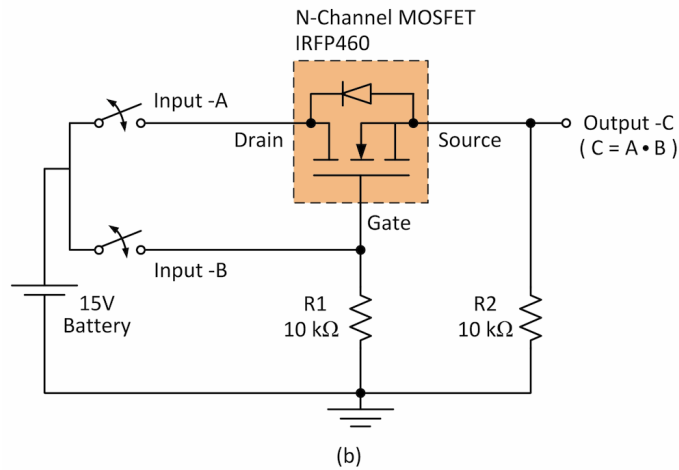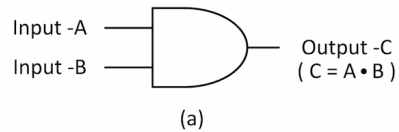
Input-A and Input-B are here connected to single pole switches that are energised from a 15V battery. Input-A is connected to the drain terminal of MOSFET; Input-B to its gate terminal. The source terminal, labelled as Output-C, is the output of the AND gate. The MOSFET in the circuit is either in cut-off or saturated mode.

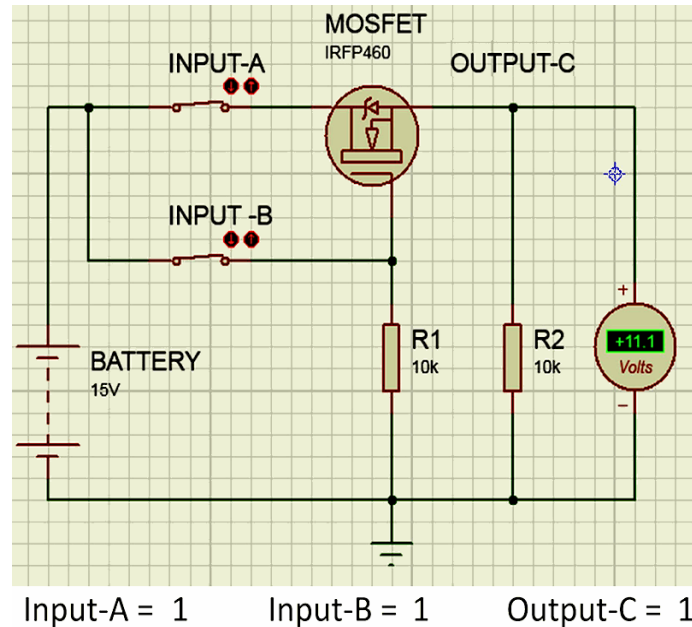When a logic-low (0V) is applied at the gate terminal, the MOSFET operates in the cut-off mode, and a high impedance is present between the drain and source terminals of the MOSFET. Similarly, when a high voltage (15V) is applied at the gate terminal, the MOSFET operates in the saturated mode, and a low impedance is present between the drain and source terminals of the MOSFET.

A NAND gate can of course be realised by adding M2 and R3 to form an output inverter.
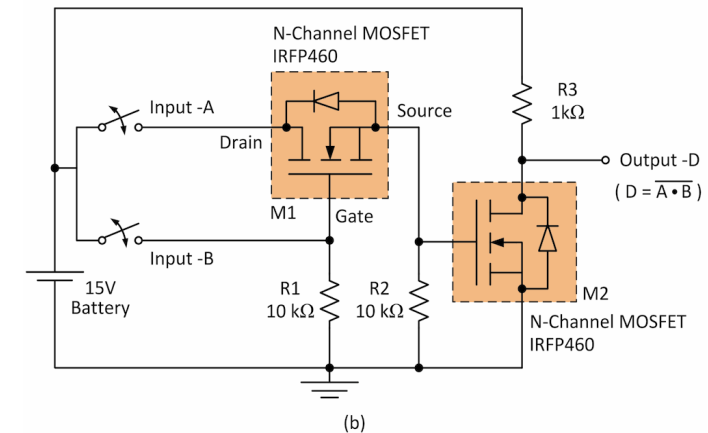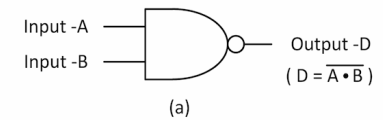

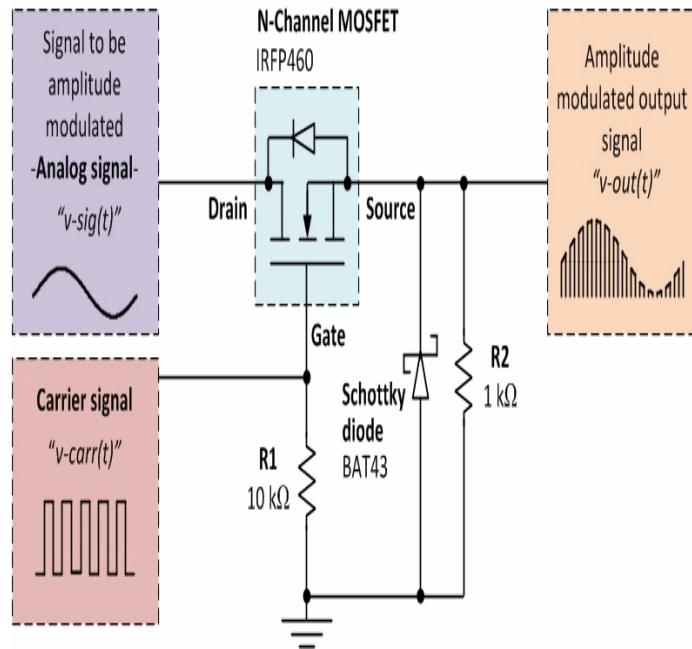**Figure 1.** *Two-input AND gate (a), and MOSFET realisation (b)*

Input-A = 1   Input-B = 1   Output-C = 1

Figure 2. *Example simulation with both inputs = 1*

Figure 3. *Two-input NAND gate (a), and MOSFET realisation (b)*

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Figure 4. *MOSFET amplitude modulator*

Figure 5. *Simulation results with a 25 kHz 12 VP-P carrier and 1 kHz 6 VP-P sine modulation*

Figure 6. *As above, with squarewave modulation*

For a more analogue MOSFET application, consider this simple AM modulator.

The circuit consists of an N-channel MOSFET, two resistors, and a Schottky diode. The modulation signal, v-sig(t), is connected to the drain terminal of the MOSFET. The carrier signal, v-carr(t), is connected to the gate terminal. The amplitude-modulated output signal, v-out(t), is obtained from the source terminal.

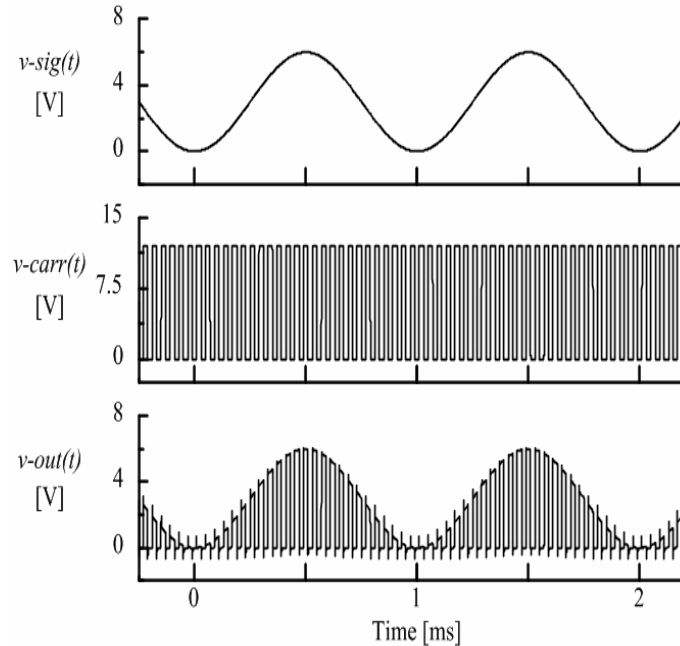The carrier signal is a square wave, and since the gate of the MOSFET is connected to the

carrier, the MOSFET will switch on and off at that frequency. When on, any voltage at the drain will pass through the MOSFET and appear at the source terminal. When the MOSFET is off, R2 will pull the output to ground.

For proper operation, the peak-to-peak voltage of the carrier signal should be twice the peak-to-peak voltage of the modulating signal. The Schottky diode prevents the amplitude-modulated output signal from being a bipolar signal.
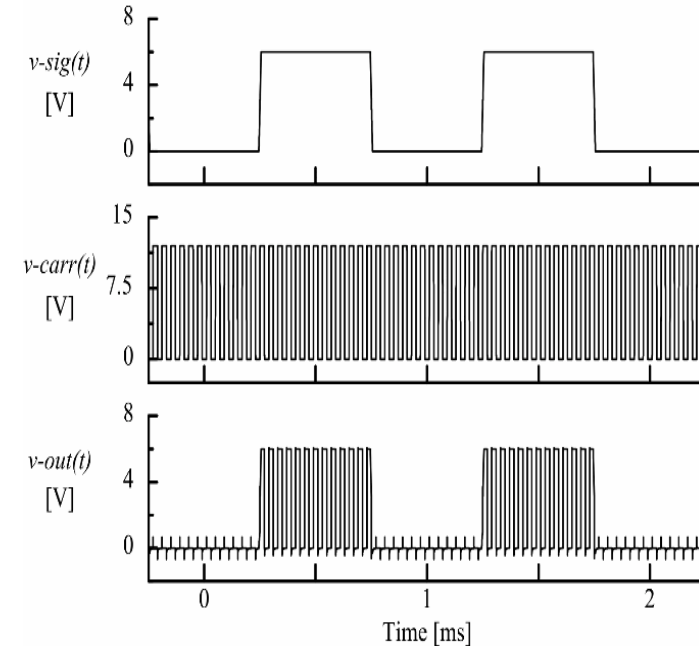
Umar Shami is an Assistant Professor in the Electrical Engineering Dept., University of Engineering and Technology, Lahore, Pakistan. He has 12 years experience of teaching and making electronic circuits especially power electronics, with interests that include driver design for power semiconductor devices, inverters, and DC DC converters.

designideas

Modded charge pump extracts power from digital signal

By Luca Bruno & Duilio Pozzoni

The voltage doubler described in this Design Idea is a modification of the Dickson charge pump. Unlike that circuit, it needs no DC input voltage, but only a digital clock whose peak value is ideally doubled at the output as a DC voltage.

The circuit acts as a charge pump, in which C1 charges to the high level of the input clock and then discharges through D2 into C2 on its low level. C2 in turn discharges into C3 through diode D3 when the clock returns high.
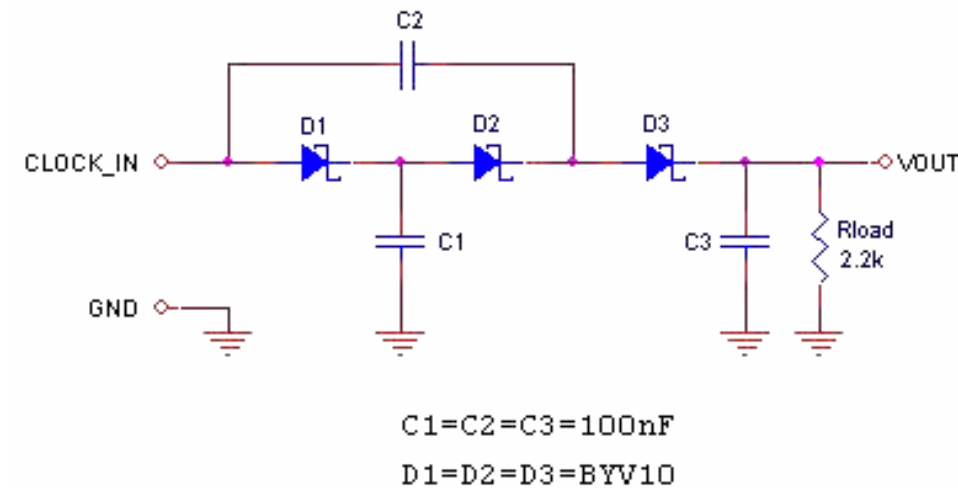
With no load, the output voltage is twice the peak input voltage, minus the forward voltage of the three diodes – about 0.75V total. The output voltage stabilises within ten clock periods; after two clocks, it reaches about 60% of the final value. Its value de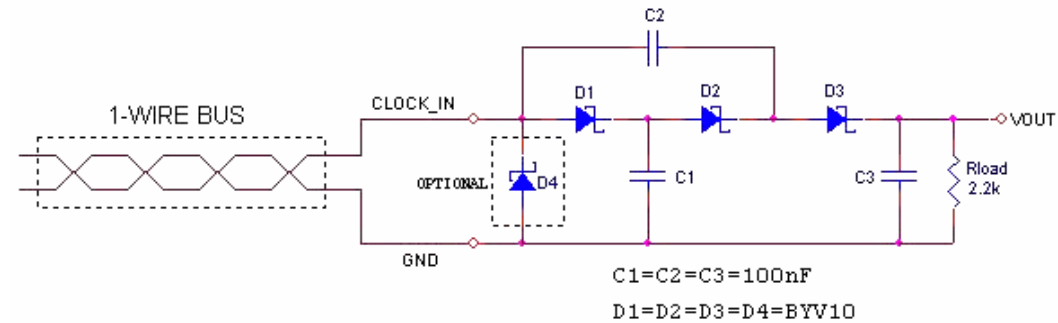pends on the load current and the peak value of the input clock, so if you want a precise output voltage you can always post-regulate.

To choose the value of the capacitors for your application you can use the following formula:

$$C = (I_{load} \times T_{low}) / V_{R\ (P\text{-}P)}$$

where I_{load} is the load current, T_{low} is the duration of the clock's low level, and $V_{R\ (P\text{-}P)}$ is the peak-to-peak ripple voltage acceptable at the output.

Figure 2. *Added anti-ringing clamp D4*

C1=C2=C3=100nF
D1=D2=D3=D4=BYV10

The circuit has been tested with a 200 kHz RC-Schmitt astable built with a 74HC14 inverter powered at V_{DD} = 5V (Figure 2). A 10m twisted cable connected the output of the astable to the voltage doubler input, and the following measurements were obtained:

RLOAD	VOUT	VR (P-P)
No load	9V	0V
2.2kΩ	8V	120mV

D4 minimises ringing on the falling edge of the input clock.

The circuit, getting power from any digital data line, can be used to provide a higher sup-

Figure 1. *Voltage doubler generates its own local V+*

C1=C2=C3=100nF
D1=D2=D3=BYV10

designideas

ply voltage in remote micropower applications not using local batteries, such as in a 1-wire serial interface network.

If you need an even higher supply voltage, you can expand the circuit to obtain an N-times multiplier. Figure 3 shows a 3-times multiplier.
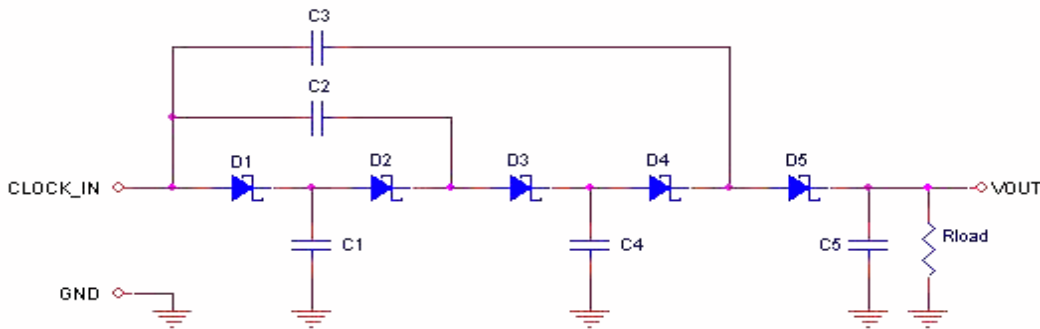

Figure 3. *Voltage tripler*

A negative voltage can also be created by inverting all the diodes and capacitively coupling and clamping the input peak to 0V. Figure 4 shows a negative voltage doubler, with the clamping circuit comprising C4 and D4. You can also obtain higher negative voltages by modifying the circuit in Figure 3.
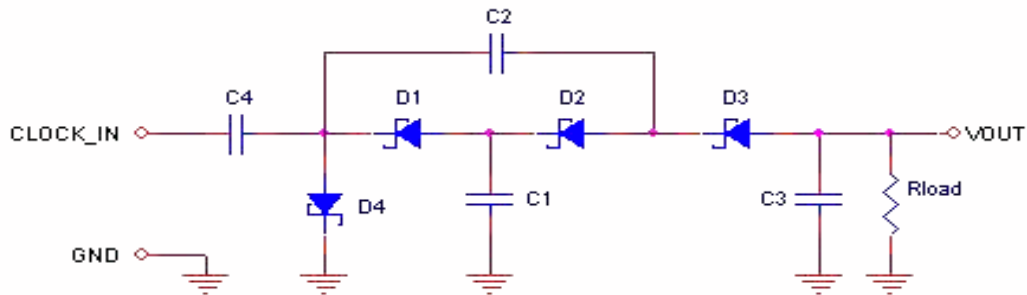

Figure 4. *Negative voltage doubler*
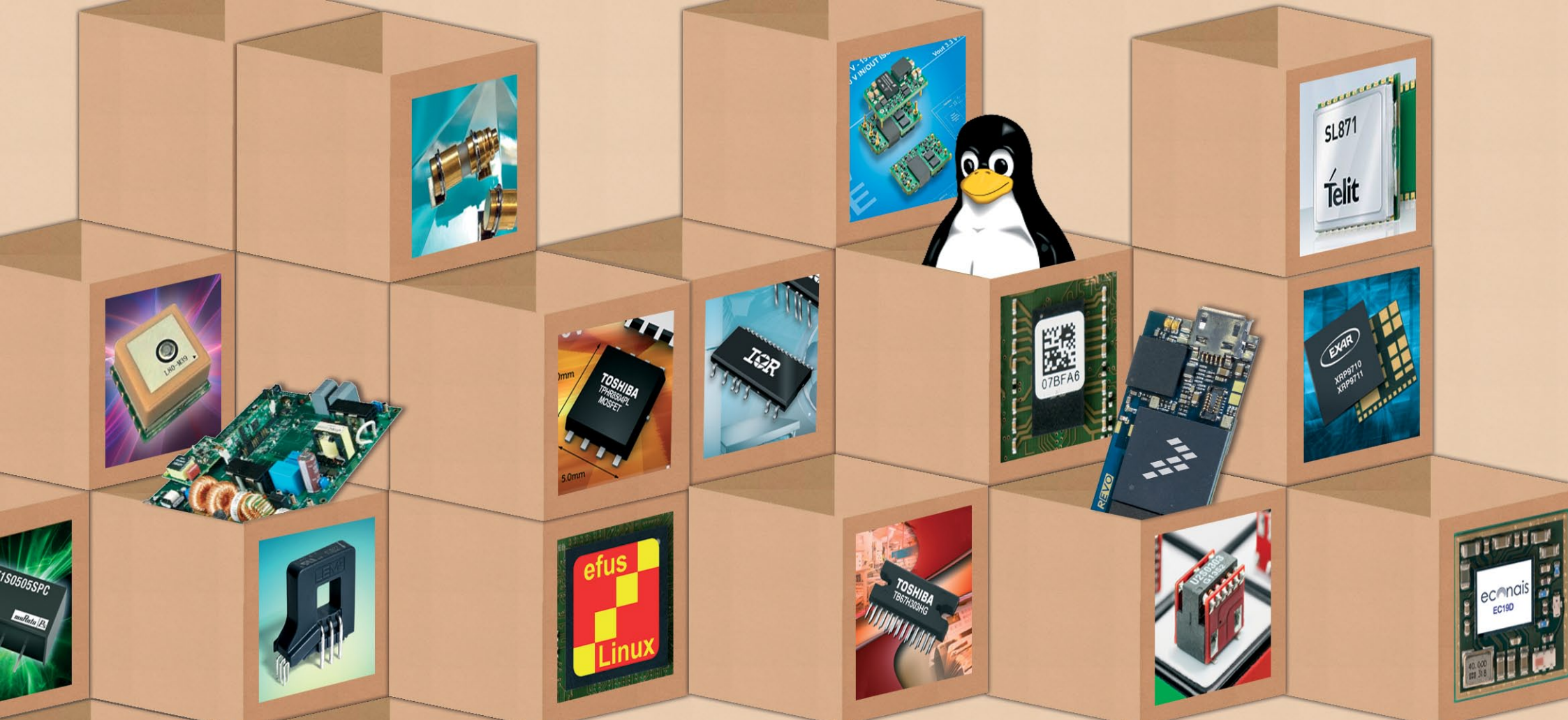
productroundup

productroundup

Vehicle comms at 5.9 GHz

Renesas Electronics has announced the R-Car W2R 5.9 GHz-band automotive wireless communication SoC for vehicle-to-vehicle (V2V) and vehicle-to-infrastructure communication (V2X). The R-Car W2R is claimed as the first device of this type capable of reducing out-of-band transmit emissions to less than –65 dBm, meeting ETSI requirements. Transmitting high-quality signals with very little interference makes it poss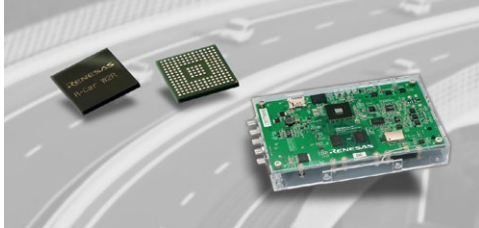ible to incorporate V2X into various types of ADAS applications, such as forward collision warning and lane keep assistance. The R-Car W2R also conforms to IEEE 802.11p.

Renesas R-Car W2R
Automotive Wireless Communication SoC for V2X

Complete article, here

Inject harmonics, test for EMI & resonance

EMI emissions and susceptibility are frequency dependent. While you can use a swept-signal generator to produce test frequencies, you may not need one. Comb generators such as the J2150A USB Harmonic Comb Injector from Picotest let you inject frequencies from 1 kHz to 1.5 GHz. It can generate impulse or square-wave signals whose frequencies are harmonics of a fundamental frequency. You can use the harmonic comb injector to look for frequencies that might interfere with your circuit's or system's operation. Furthermore, you can perform spectrum testing on clocks and power-distribution networks.
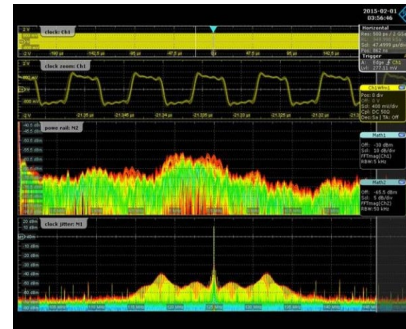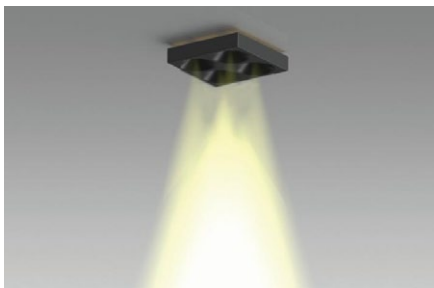
Complete article, here

"Chip-scale optics" shapes LED light patterns

Plessey Semiconductors has developed technology for Chip Scale Optics (CSO) based on its GaN-on-Silicon MaGIC LEDs. Chip Scale Optics permits design of light emission angles down to ten degrees direct from the LED, enabling significant reductions in cost of lighting fixtures. Plessey realised that the original growth silicon, normally sacrificed during LED production, could be shaped and used to form mechanically robust, MEMS-type features on the emitting surface of a vertical LED. Having the primary optics on-chip eliminates the cost of primary optics typically found in packaged LEDs and chip-on-board modules.

Complete article, here

Customisable circular OLED module

Custom and semi-custom display specialist andersDX has extended its range of Circular Display Modules with the addition of a round OLED display module. The 1.13-in. (2.87 cm) Passive Matrix OLED TFT Display is again targeted at wearable electronics, especially in the healthcare and fitness sectors, and is manufactured by Truly Semiconductor (Hong Kong). The module is fully customisable and also offers an attractive option in a number of industrial applications. The OEL9M0082-W-E PMOLED has an active area of 28.8 x 28.8 mm and a resolution of 128 x 128 dots.

Complete article, here

productroundup

Microchip continues 8-bit MCU platform growth

With this expansion of its development platform for Microchip's portfolio of 8-bit PIC microcontrollers (MCUs) with Core-Independent Peripherals (CIPs), designers can combine these building blocks to perform application functions autonomously, and they can be interconnected with an increasing number of integrated 'Intelligent Analog' peripherals. Because these functions are deterministically and reliably performed in hardware instead of software, CIPs enable system performance that is far beyond traditional MCUs.
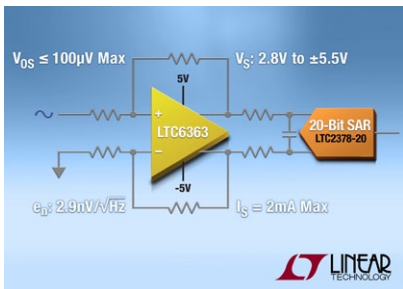
Complete article, here

Boost ADC performance at Gsample rates

Swedish company Signal Processing Devices' digital time-interleaved ADC mismatch error correction IP-core for FPGAs is used to enhance ADC performance, and the company has published figures for improved results obtainable with three off-the-shelf ADCs from leading semiconductor manufacturers. When time-interleaving several ADCs, differences in gain and phase-response (including time-skew), as well as DC offset between the individual ADCs, produce nonlinear distortion (aliasing) that is typically the main performance limitation of time-interleaved ADC arrays. These differences are usually referred to as mismatch errors and are very challenging to remove by purely analogue design [refinements] and careful circuit layout. With digital mismatch error correction the mismatch errors can be handled even when the errors vary over frequency: unwanted aliasing spurs are suppressed down to the noise floor.

Complete article, here

Precision differential amp drives 20-bit ADCs, uses 2 mA

LTC6363 is a low power, high precision, fully differential amplifier intended for driving high performance 16-, 18- and 20-bit SAR and ΔΣ ADCs. With 100 µV maximum input offset voltage and 2.9 nV/√Hz input-referred voltage noise, the LTC6363 consumes 19 mW on a 10V supply. It can convert single-ended signals to differential outputs or be used in a fully differential manner, settling an 8 VP-P differential output step to 18-bit resolution in 780 nsec. Four external resistors set the amplifier's gain; LT5400 highly matched quad resistors can be used to boost linearity.

Complete article, here

Isolation amp includes ΔΣ ADC

For current sensing and voltage sensing in power converters, these photocouplers achieve high accuracy through the inclusion of a delta sigma analogue-to-digital converter (ADC). The TLP7820 and TLP7920 are analogue output type devices; digital output variants will be added. To deliver extremely accurate feedback to a microcontroller on status of the phase current of the motor or the variation of the bus voltage, Toshiba has equipped its newest photocouplers with a delta sigma ADC at the input side that enables the devices to achieve a high level of linearity (0.02% @NL200, typical).

Complete article, here

productroundup

Matrix sensors; "next-generation HMI experience"

Peratech's Opaque QTC force touch sensors offer HMI possibilities for automotive designers and engineers, the company believes. The slimline, infinitely customisable sensor system and complementary firmware address what Peratech sees as the failings of capacitive sensing whilst enabling next generation design themes, user experience, packaging benefits, and safety. QTC-based sensors can be integrated under a wide range of top surfaces and under flexible and rigid displays. With a wide force-sensing range and electronically-configurable force thresholds, QTC-based sensors eliminate false touches.
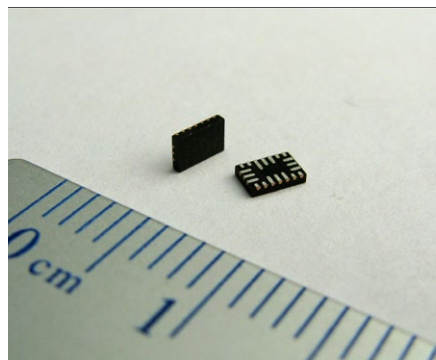
Complete article, here ▶

Mixed-signal IC interfaces voltage domains

Silego Technology's 17-GPIO SLG46621V GreenPAK4 programmable mixed-signal IC features dual supply capability allowing designers to flexibly interface two independent voltage domains in their design using the programmable logic, timing, and analogue components available on all Green-PAK4 family devices. The SLG46621V introduces dual supply GPAK products to the Silego range, and features an 8-bit SAR ADC, six analogue comparators, plus logic and timing resources. The SLG46621V is available in a 2.0 x 3.0 x 0.55 mm 20-pin STQFN.

Complete article, here ▶

Imagination highlights virtualisation in 32-bit PICs

Following Microchip's announcement of its PIC32MZ microcontrollers, Imagination Technologies, supplier of the MIPS core around which the PICs are built, is emphasising that the MIPS M-class CPUs concerned are the only microcontroller-class CPUs to feature full hardware virtualisation. The Microchip PIC32MZ integrates the MIPS M5150 CPU, Imagination's latest Warrior M-class processor. Virtualisation enables users to run multiple operating systems or applications on a single physical machine; MIPS M-class CPUs bring this feature from the desktop and server world into a microprocessor that is 25x-50x smaller than conventional mobile chips. A MIPS M5150 CPU, Imagination adds, can run up to seven guest operating systems in parallel, with minimum overhead on overall system performance and stability. The company believes this will contribute to innovative applications for wearables, IoT and other embedded markets.

Complete article, here ▶

Tiny DC/DC converters output up to 10kV

Housed in miniature 1.0 × 0.5 × 0.5-in. plug-in packages, unregulated DC/DC converters in Pico's AVP/AVN series deliver output voltages of 6 kV to 10 kV at 1.25W. These devices, which were originally designed for a space platform application, are now available as standard products with a choice of five input voltages and either positive or negative output. The single-output converter modules operate over a temperature range of -25°C to +70°C with no heat sink or electrical derating. An expanded temperature range of -55°C to +85°C is optional, as is environmental screening to MIL-STD-883.
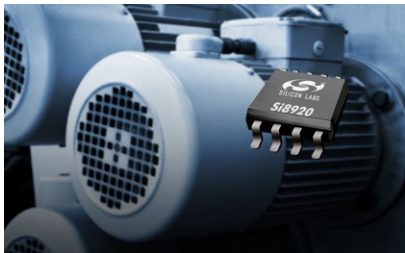
Complete article, here ▶

productroundup

Fast isolated current sensing

Silicon Labs says it has the fastest-available isolated current sense amplifier in the Si8920 analogue amplifier, offering precise current shunt measurement for power control systems including industrial motor drives and inverters. Measuring current on high-voltage rails (up to 1200V), the Si8920 isolated amplifier provides a differential, low-voltage input scaled for connection to current shunt resistors, enabling the controller to make precise measurements of current while maintaining electrical isolation. The device's signal bandwidth (up to 750 kHz) ensures rapid, precise dc current measurement and accurate representation of the primary signal and harmonics.

Complete article, here

Near-field probe measures fields to 10 GHz

The high measurement resolution of the SX probe heads from Langer EMV-Technik allows the developer to pinpoint RF sources of between 1 GHz and 10 GHz on densely packed printed circuit boards or on IC pins. The latest SX1 near-field probe set contains three near-field probes with high resolution for measurements in the upper frequency range; an E-field probe for frequencies between 1 GHz and 10 G; an H-field probe for frequencies between 1 GHz and 10 GHz with a very small probe head; and the SX-B 3-1 H-field probe for frequencies between 1 GHz and 3 GHz whose measurement coil is arranged orthogonally to the probe shaft. The near-field probes are connected to the 50-Ohm input of a spectrum analyser or oscilloscope via a shielded cable and SMA connector during the measurement. The near-field probes have an internal terminating resistor.

Complete article, here

Quick-start kit packages BLDC vector control

With STMicroelectronics' STM32 Motor-Control Nucleo Pack, you can "plug and spin" brushless DC motors in, "just a few seconds" - the company promises. The $35 starter kit plus free-of-charge software algorithm aims to help engineers and hobbyists implement efficient vector control in a very short time for motor-driven projects such as drones, appliances, E-bikes, home-automation, health care, and industrial machinery. The pack contains an STM32 F3 Nucleo microcontroller board, plug-in 48V/1.4A motor-driver board based on the STSPIN L6230 motor-driver IC, and a low-voltage brushless motor.
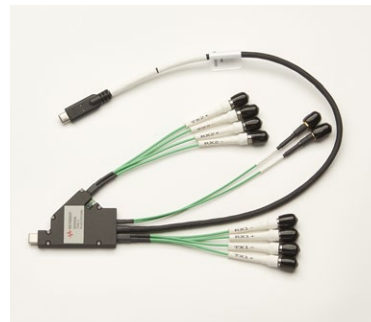
Complete article, here

Type-C interconnect test fixtures major on signal integrity

To assist engineers verify and debug devices that use Type-C connector technology, Keysight Technologies has designed what it claims to be the highest-signal-integrity Type-C test fixtures for high-speed differential bus probing. As well as USB, the connector may be used with standards such as DisplayPort, Thunderbolt and MHL. The N7015A high-speed test fixture provides up to 30 GHz bandwidth, enabling engineers to verify and debug USB 3.1 Gen 2 designs: and designs using other high-speed signal standards that support the Type-C connector.

Complete article, here

CONNECTIONS

MICRO-USB FAILURE LEADS TO A USB POWER ADAPTER EDUCATION   BRIAN DIPERT, EDN

The most innocuous of glitches sometimes blossom into much bigger engineering exercises and educational opportunities. The other day, I was out on the back deck reading, A Game of Thrones, volume one of the A Song of Fire and Ice series, to be precise, using the Kindle app on my Google Nexus 7 (2013 edition) tablet. Bright sunlight washed out the LCD, so I went inside to get my Kindle Keyboard as an alternative. My aspirations were thwarted, however, by the e-book reader's completely drained battery.

Its companion USB-to-micro-USB charge cable was buried deeply in my attaché case, so instead I grabbed a Samsung-branded 5-ft. cable I'd recently bought, which was sitting on my desk. I plugged it into an Apple 10W USB power adapter I also had handy, and ... nothing.

The amber (when charging, green when done) LED on the bottom of Kindle Keyboard didn't illuminate, and the E Ink display also didn't indicate that anything encouraging was happening. I also tried the Samsung cable-plus-Kindle Keyboard combo with two multi-port USB chargers; an Orico DCT-5U, which offers both 1A and 2A output options, along with an OTG (on-the-go)-compatible port pair:

And a Sabrent AX-U5PB, which is supposedly able to deliver 2A to each of its five USB ports:

None of the ports on either of the chargers did the trick, leading me to suspect that I had a bad cable on my hands. However, on a hunch, I connected the Samsung cable to my two Android smartphones, a HTC One M7 and a first-generation Motorola Moto X ... and they both happily reported that they were charging just fine, using all three power adapters, and across both current-output options on the multi-port units.

Had my Kindle Keyboard died? No, it charged fine using the cable it originally came with, after I dug it out of my bag. Well then, was there something special about this particular cable? No again; the other four Samsung-branded generic cables I'd bought at the same time worked fine. Something was amiss with *this particular Samsung cable* – for the *Kindle Keyboard in particular*. [Retailer] A4C is in the process of replacing the cable as I write these words, but I was still intrigued.

What I learned hasn't led to any definitive conclusions, but it's certainly bolstered my respect for designers of USB power adapters, along with those of the devices whose batteries get recharged. First off, as a reminder, the USB hardware standard is nominally a four-shielded-wire configuration: a twisted pair for half-duplex differential data (USB 3.0 adds two more twisted pairs, for full-duplex and higher-speed support), 5V power, and ground. Micro-USB connectors add a fifth "ID" pin for OTG support, grounded at the host and left floating at the device.

I'd initially suspected that the Samsung cable's 5V wire might not be supplying adequate current to charge the Kindle keyboard. And indeed, the gauge of wire used can notably affect both charging speed and data transfer bandwidth; well-known consumer electronics review site The Wirecutter specifically tests for and rates cables based on these particular parameters. But given that both of my Android smartphones are happily charging away (and with no slow-charge warning pop-up messages) using this exact same cable, I doubt the 5V wire is the fundamental culprit. Some of the Internet

CONNECTIONS

coverage on the topic references wire gauge markings on the cable jacket; my cable doesn't have this, but the following alphanumeric pattern (with ??? referencing an unknown-to-me symbol) is repeated several times along its 5-ft. length:

B239426-C5 ??? AWM 21100 80°C 30V VW-1 ...... C??? I/II A 80°C 30V FT1 HONGLIN NON-PVC

I was also already conceptually aware that chargers and devices conducted an initial negotiation process upon first connection-via-cable to determine the device's maximum-accepted current draw needs versus the charger's maximum-possible current output. I'd thought that

this handshake was analogue (and 5V wire-based) in nature; the device would measure whether the charger could source the maximum current that the device "sink" could accept and, if not, would assess and adjust based on the (lower) amount of current that was available.

The data wire-based reality is more complicated and explains why I've also experienced a few other charger-plus-cable-plus-device combination non-starter situations in the past. I quote:

Device makers being a competitive lot, there's no one standard negotiation – it's a bit like having to speak six languages.

Apple started it with the iPhone – since the original USB specification had no standard for high-speed battery charging, Apple came up with its own 'electrical signature.'

It decided that if an iPhone or iPad came up against a USB port with 2.0VDC on the D+ line and 2.7VDC on the D- line, that port would be an Apple iPhone (DCP) charger that could supply 1000 mA of current. If the voltages were reverse (2.7V/2.0V on the D+/D- lines), it'd be an iPad charger with 2000 mA maximum supply.

But it didn't end there. While the USB forum released a generic 'signature' standard, other manufacturers came up with their own signatures and in the end, there are at least six D+/D- signatures in the wild:

2.0V/2.0V – low power (500 mA)
2.0V/2.7V – Apple iPhone (1000 mA/5W)
2.7V/2.0V – Apple iPad (2100 mA/10W)
2.7V/2.7V – 12W (2400 mA, possibly used by Blackberry)
D+/D- shorted together – USB-IF BC 1.2 standard
1.2V/1.2V – Samsung devices

These days, resistance-based voltage sensing options like the first four are described as 'legacy' modes and all new devices we believe use chip-based detection.

However, with millions of 'legacy' devices (and even more AC chargers) in the wild, they still have to be accounted for. Chips like Texas Instruments' TSP2514 and TSP2543, Microchip's USB2534, and ST Microelectronics STCC5011 all handle these various signature combos.

So if I had to hazard a guess, it'd be that one of the two data lines has gone awry, either with higher-than-desired resistance (magnified by the cable's generous 5 ft. length), a complete open circuit, or a short-circuit to its peer. The Android smartphones handle the altered-wire situation without a hiccup, but the Kindle Keyboard doesn't see what it's looking for and completely balks at the charge attempt. I suspect that if I tried to use the misbehaving cable to transfer data to or from one of the Android handsets, versus to charge them, my results wouldn't be positive with these platforms, either.

EDN europe

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